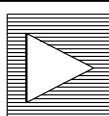
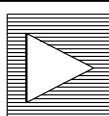
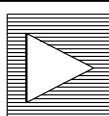
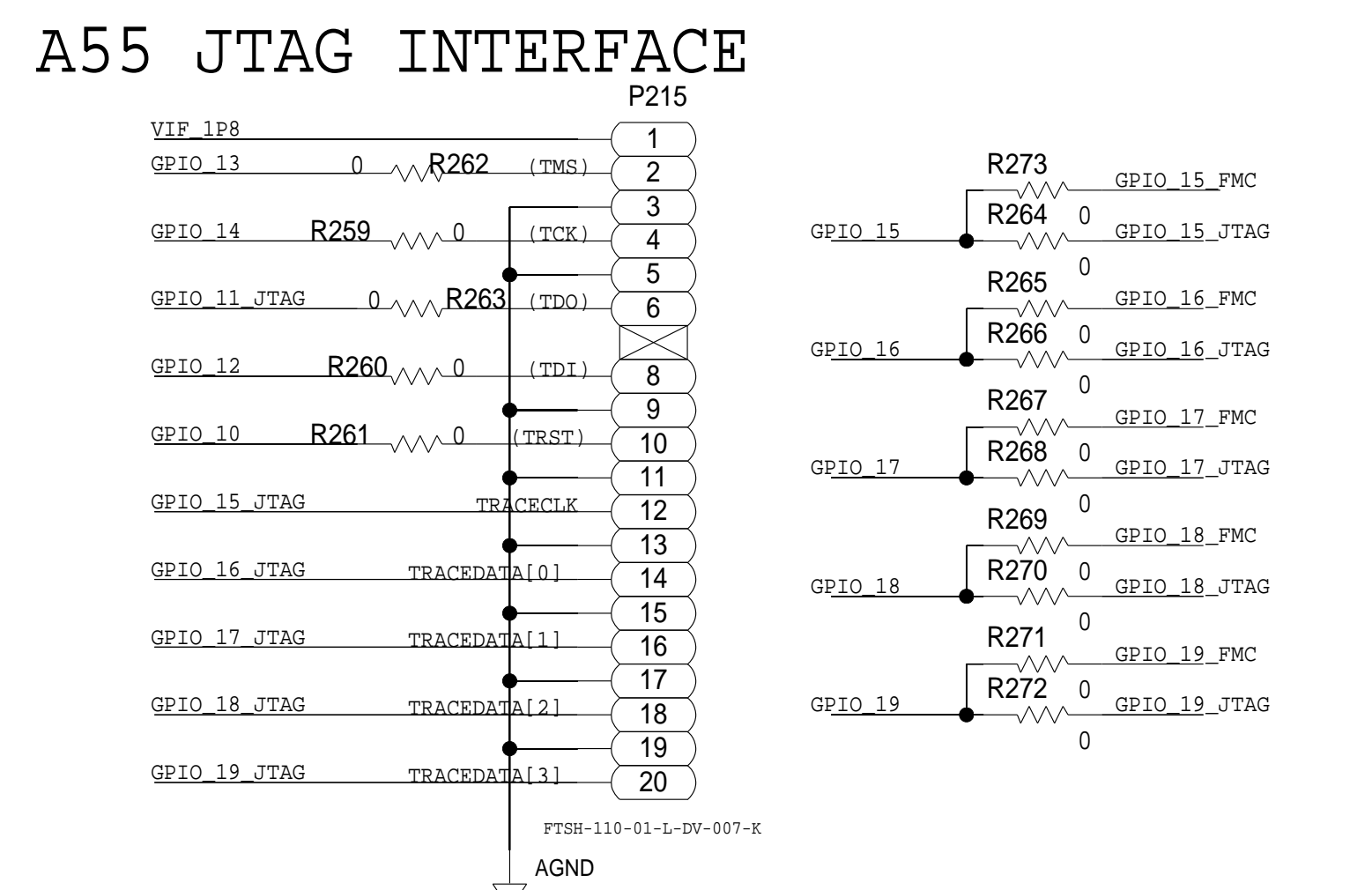
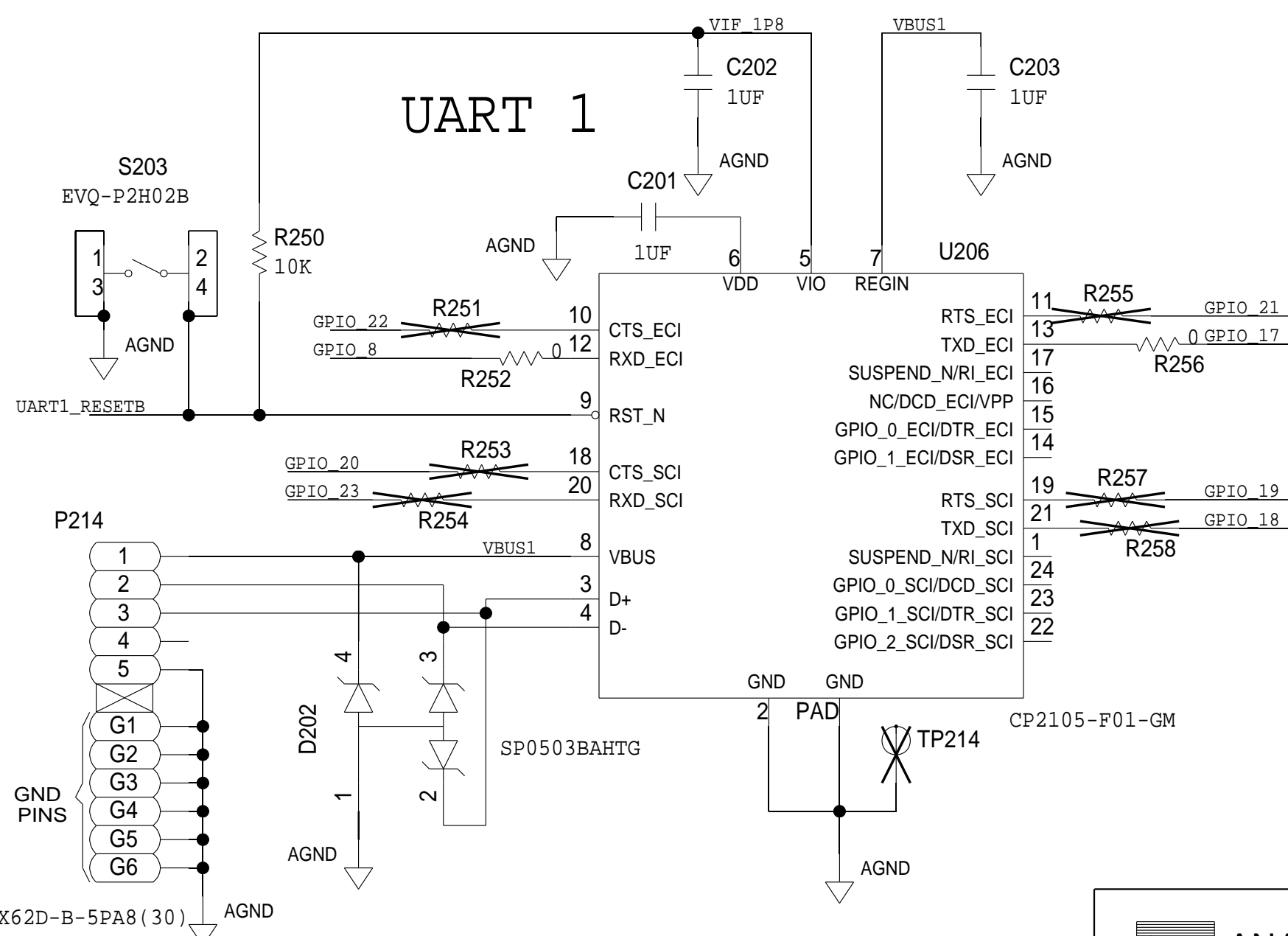
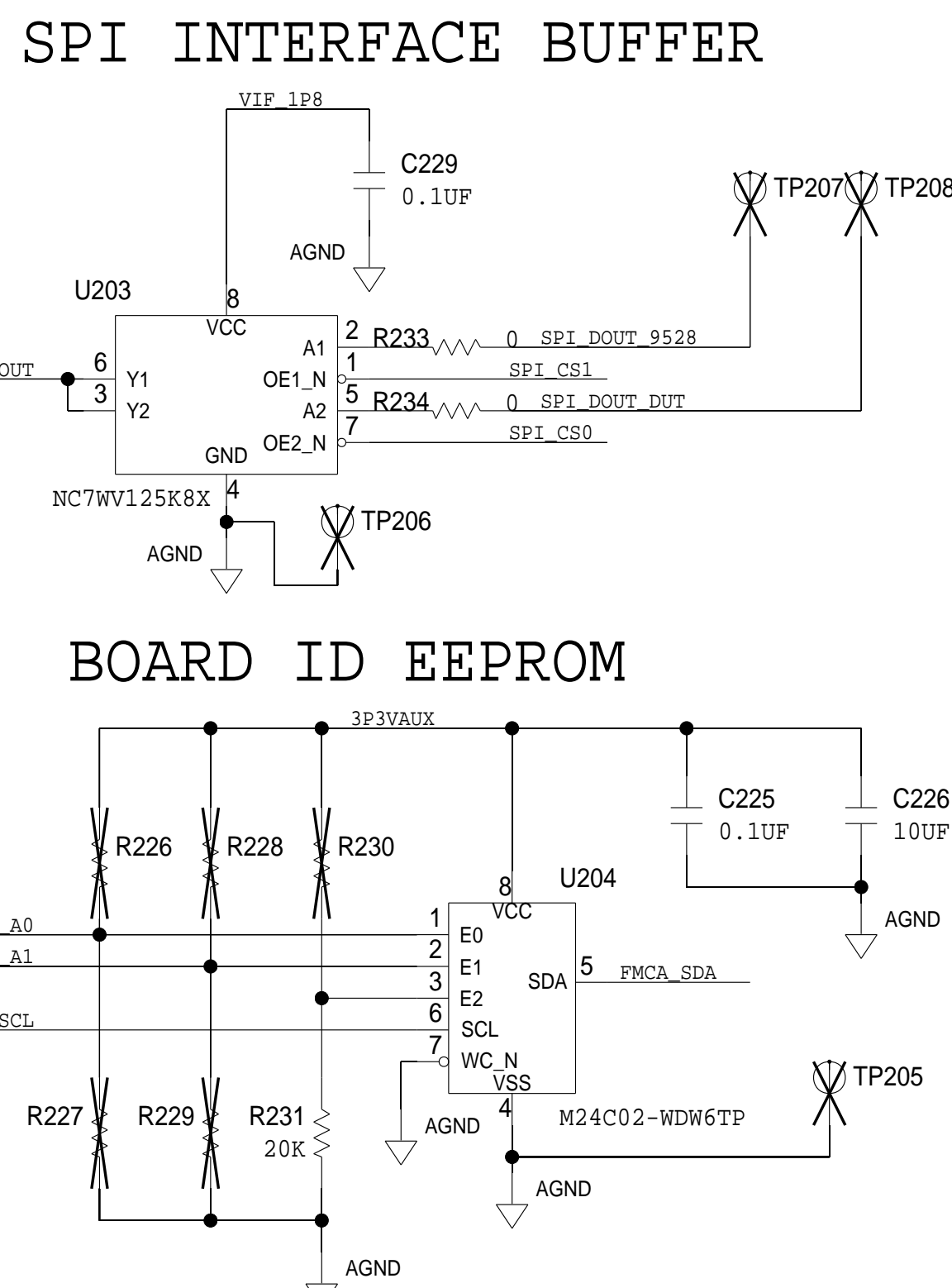
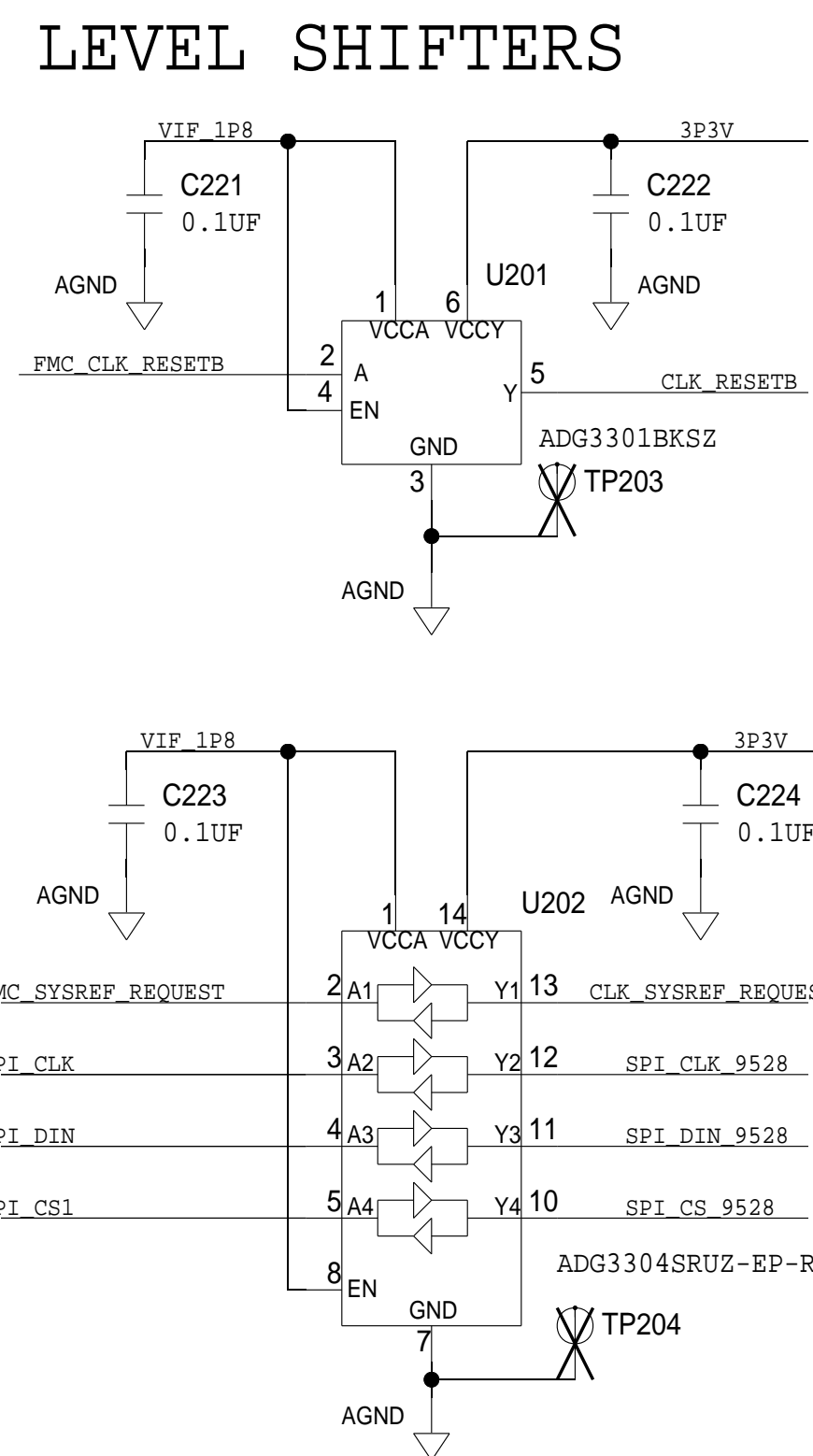
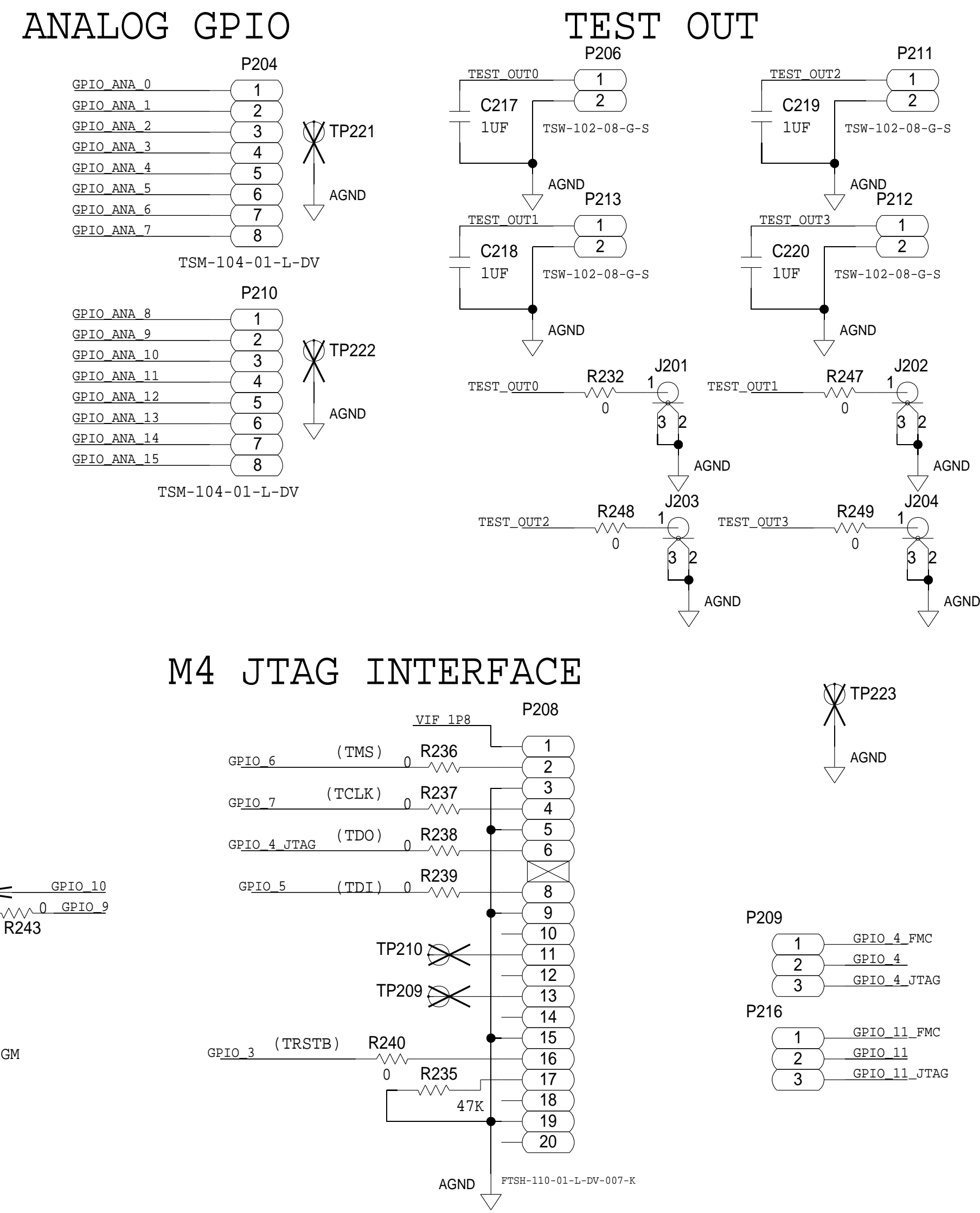
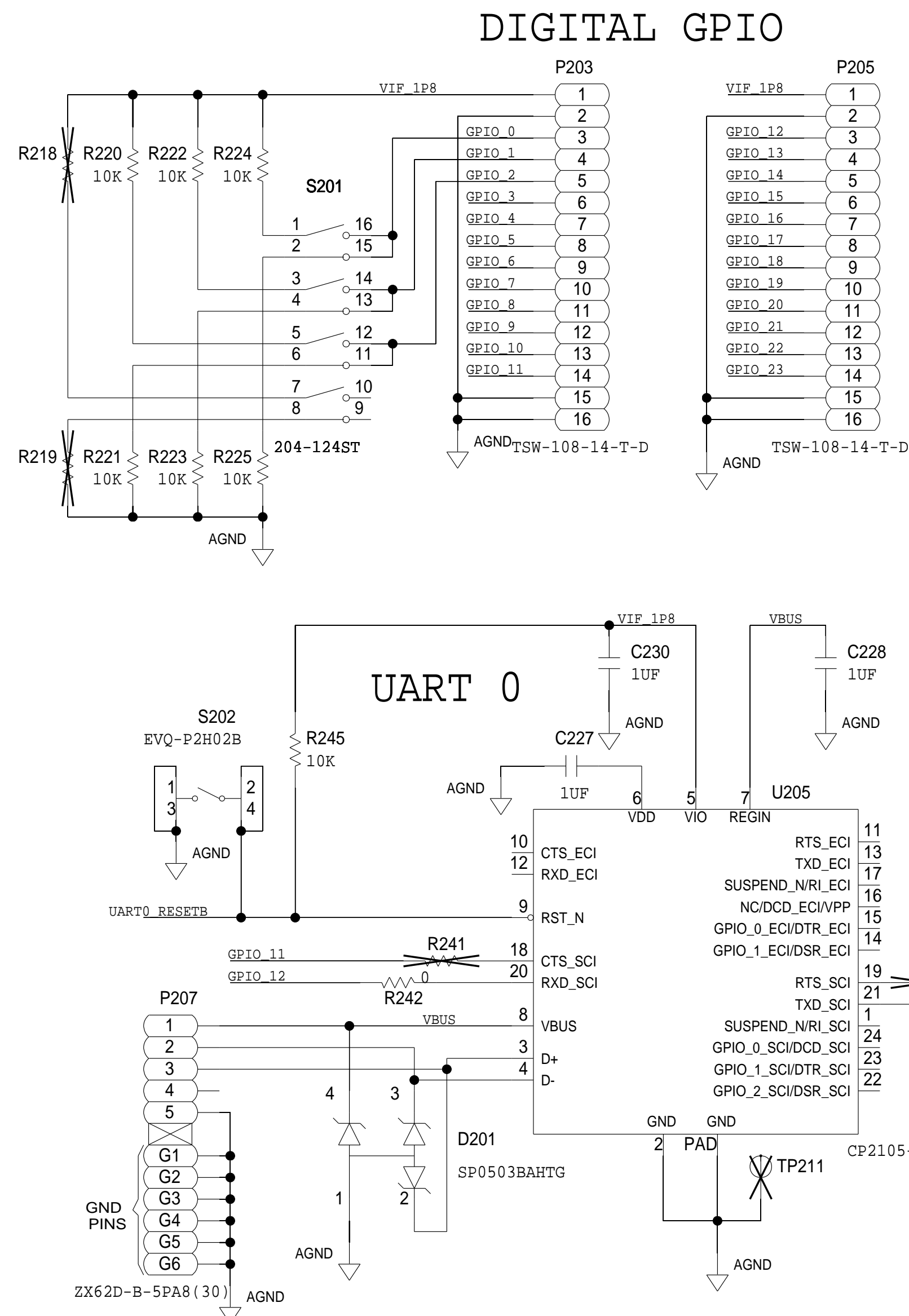
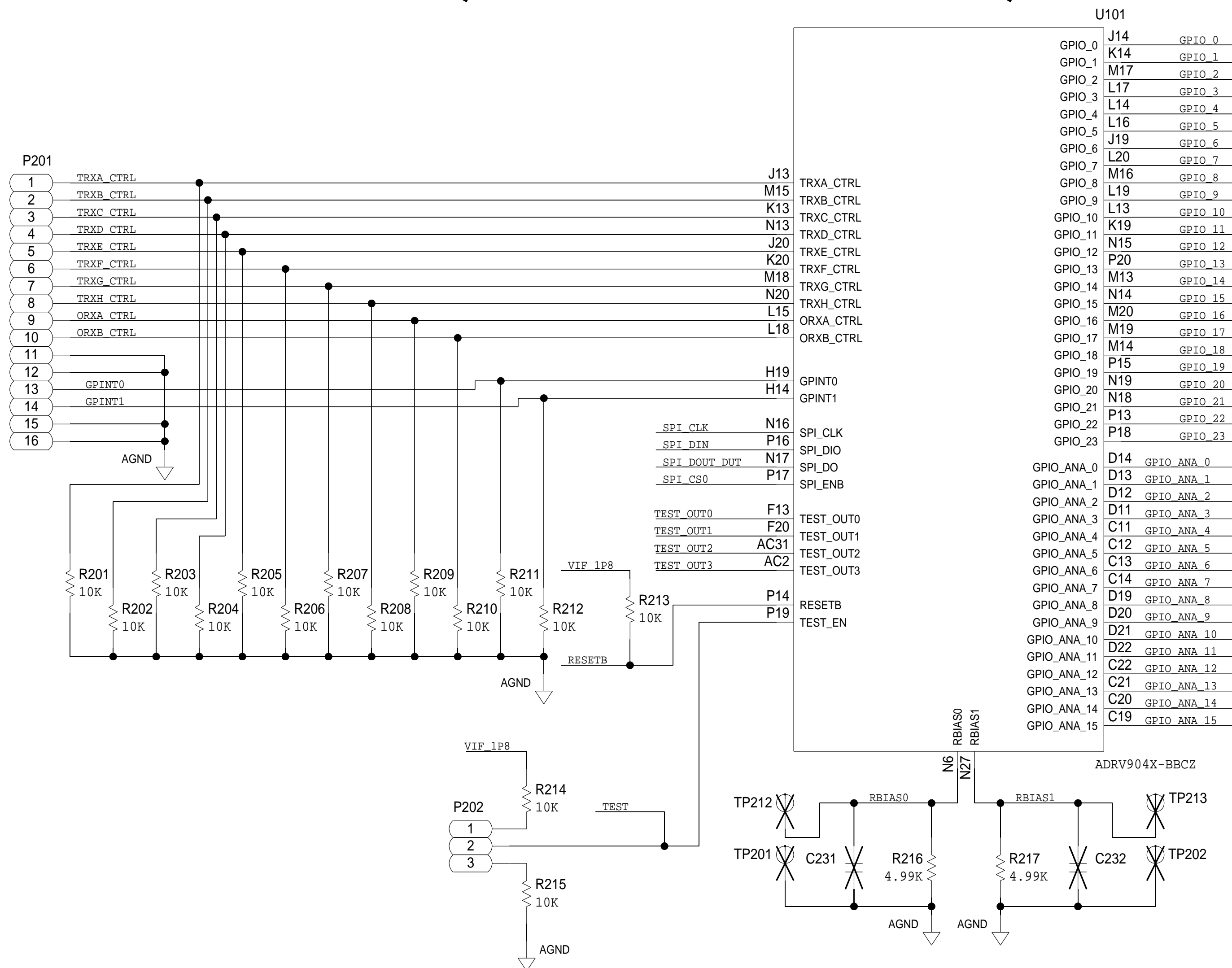



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DIGITAL / ANALOG I / O

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

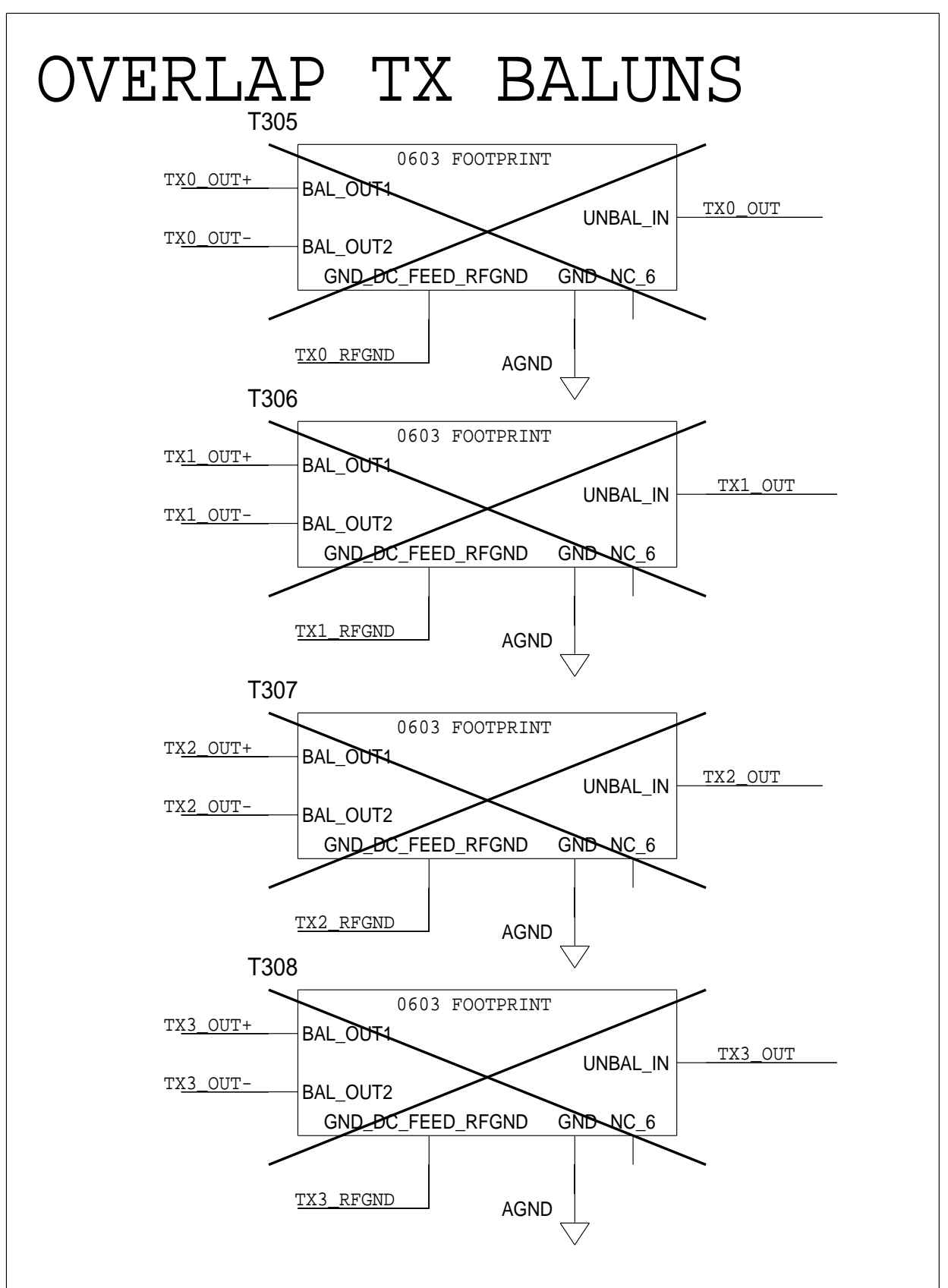


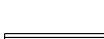
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	HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A				
<div>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETERMINED TO BE IN THE INTERESTS OF ANALOG DEVICES. THE EQUIPMENT DESIGN HEREON MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY ANALOG DEVICES.</div>	DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_066795		REV C
	PTD ENGINEER <PTD_ENGINEER>		SIZE D	SCALE 1:1	SHEET 2 OF 19

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

U101		
TX0N	B1	TX0-
TX0P	C1	TX0+
TX1N	G1	TX1-
TX1P	H1	TX1+
TX2N	R1	TX2-
TX2P	T1	TX2+
TX3N	AA1	TX3-
TX3P	C32	TX3+
TX4N	B32	TX4-
TX4P	H32	TX4+
TX5N	G32	TX5-
TX5P	T32	TX5+
TX6N	R32	TX6-
TX6P	AA32	TX7-
TX7P	Y32	TX7+

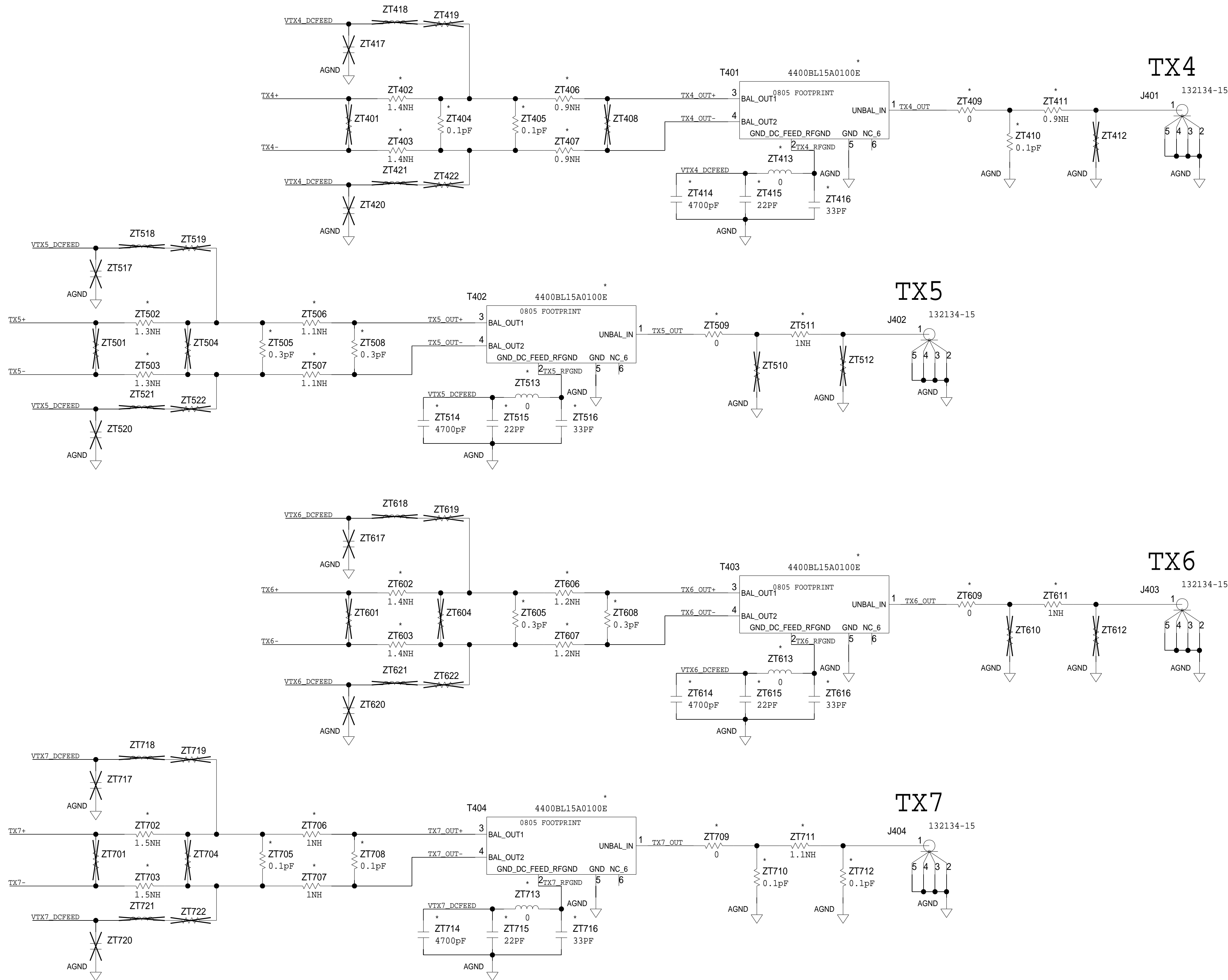
ADR9V04X-BBC2



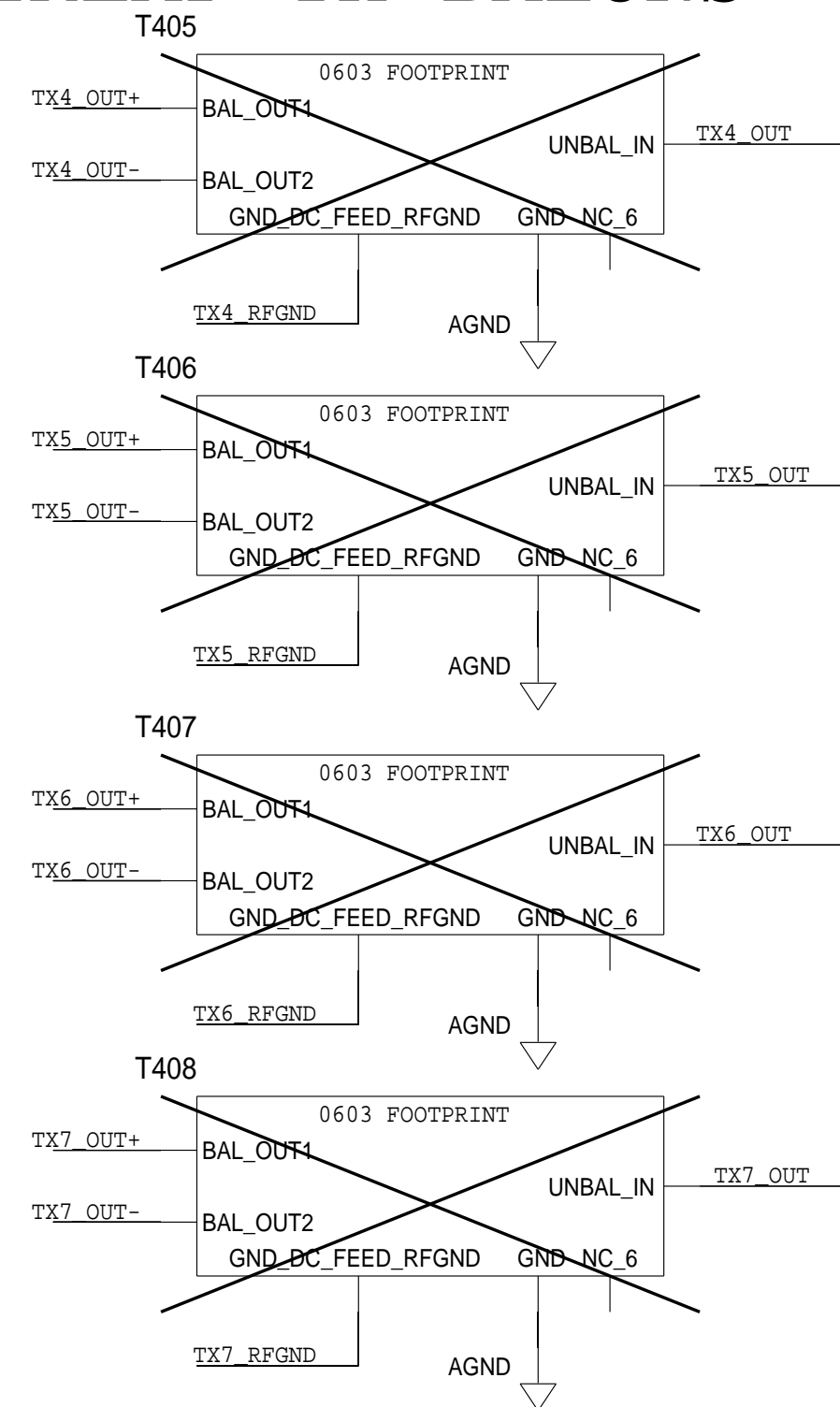
<div>ANA LOG DEVICES</div>	SCHEMATIC				
	HW TYPE : Customer Evaluation Product(s) : ADRV904X N/A				
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	PDT ENGINEER <PDT_ENGINEER>		SIZE 1:1	SHEET 3	OF 19

TRANSMITTER RF OUTPUT

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.



OVERLAP TX BALUNS



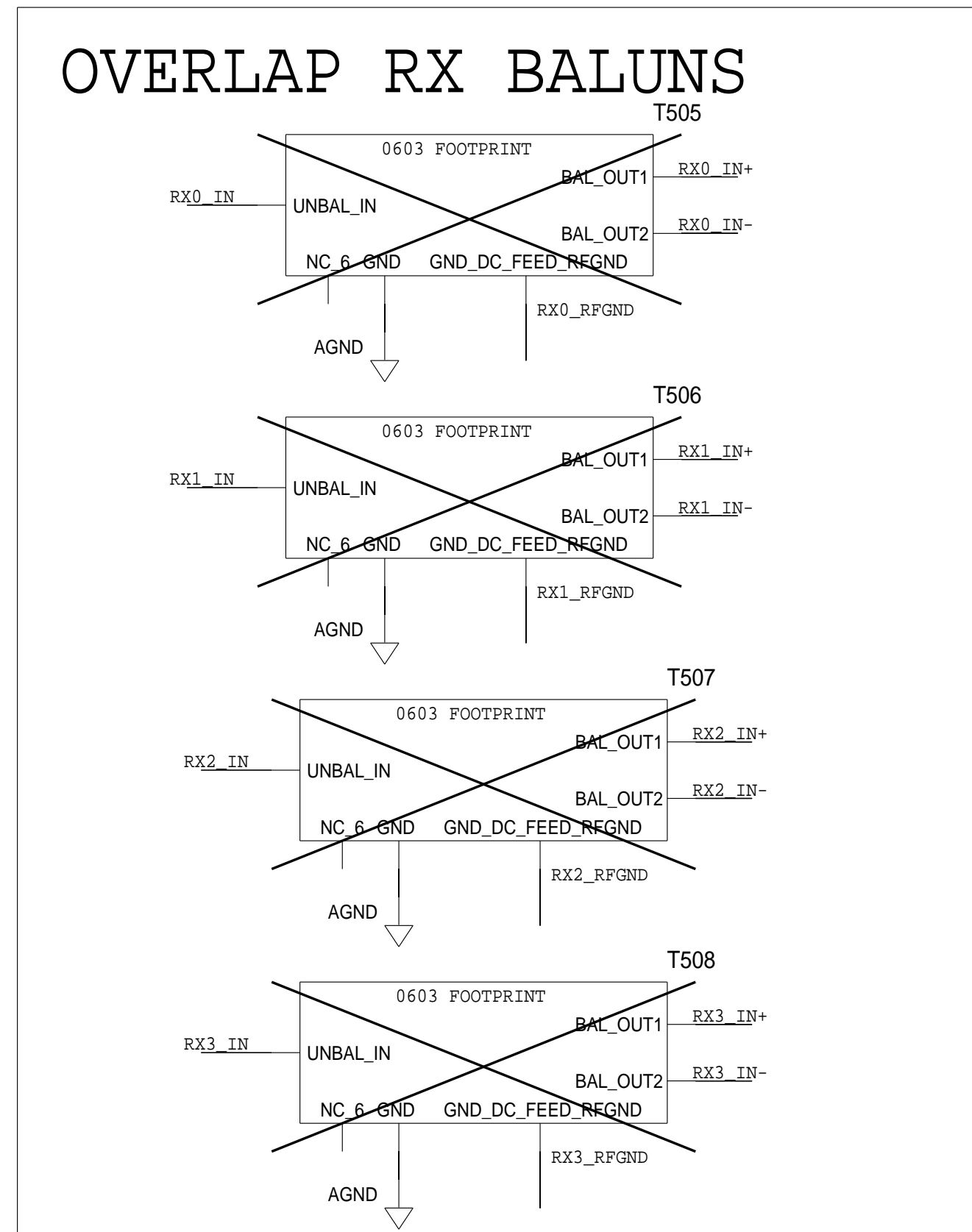
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OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS
OF ANALOG DEVICES.
THE EQUIPMENT SHOWN HEREON MAY BE PROTECTED BY PATENTS
OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.


SCHEMATIC				
HW TYPE : Customer Evaluation Product(s): ADRV904X : N/A				
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795		REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 4	OF 19

EV6 MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

		U101
RX0 -	D4	RX0N
RX0+	C4	RX0P
RX1 -	J4	RX1N
RX1+	H4	RX1P
RX2 -	P4	RX2N
RX2+	N4	RX2P
RX3 -	W4	RX3N
RX3+	V4	RX3P
RX4 -	C29	RX4N
RX4+	D29	RX4P
RX5 -	H29	RX5N
RX5+	J29	RX5P
RX6 -	N29	RX6N
RX6+	P29	RX6P
RX7 -	V29	RX7N
RX7+	W29	RX7P

ADRV904X-BBC2



 ANALOG DEVICES	<h1 style="text-align: center;">SCHEMATIC</h1>				
	HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A				
<small>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSE DETRIMENTAL TO THE INTERESTS OF ANALOG DEVICES. THIS EQUIPMENT DESIGNATION MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OWNED ANALOG DEVICES.</small>	DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_066795		REV C
	PTD ENGINEER <PTD_ENGINEER>		SIZE D	SCALE 1:1	SHEET 5 OF 19

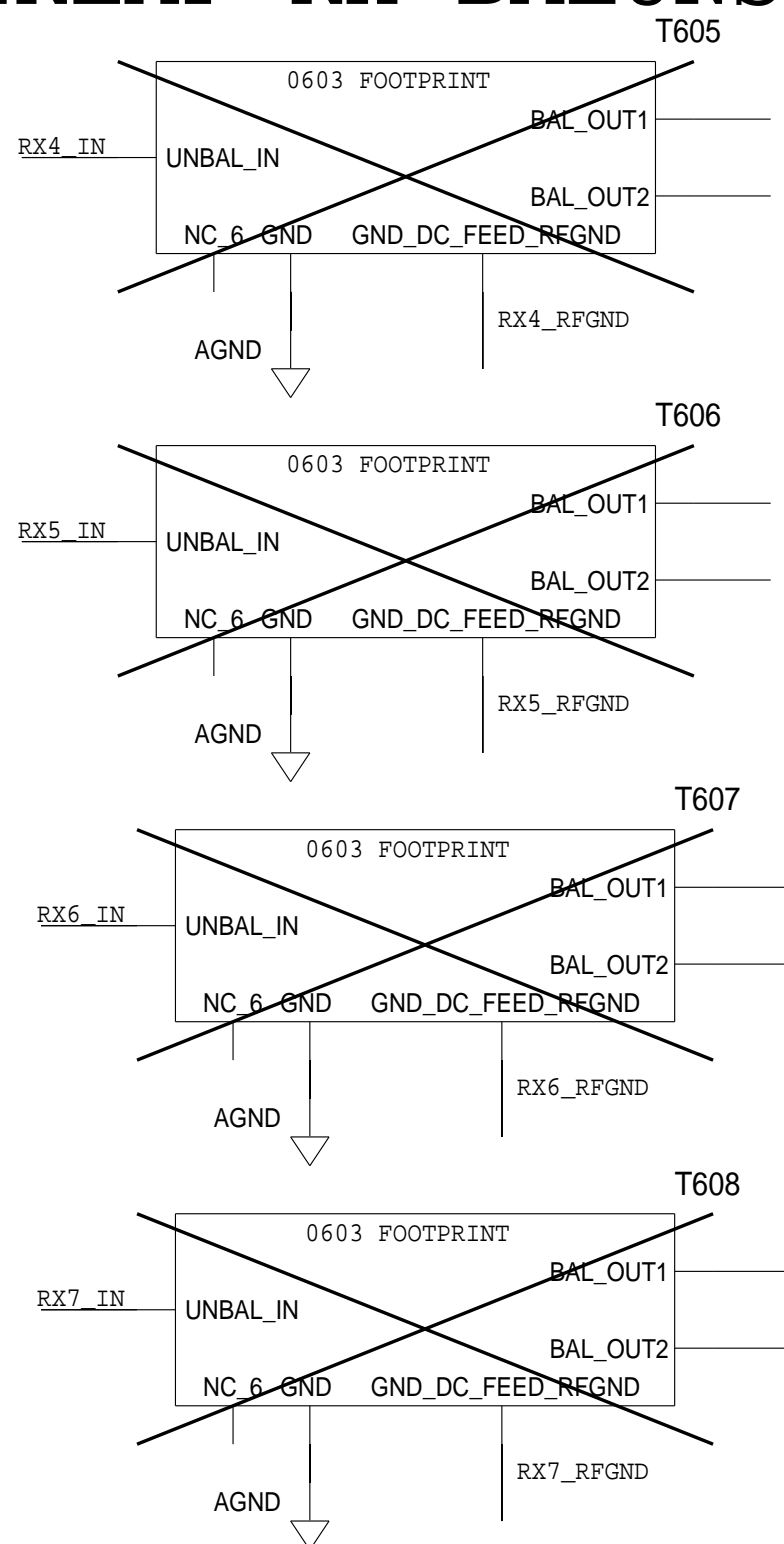
RECEIVER RF INPUT

EVB MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



OVERLAP RX BALUNS



SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): ADRV904X
: N/A

DESIGN VIEW
<DESIGN_VIEW>

DRAWING NO.
02_066795

REV
C

PTD ENGINEER
<PTD_ENGINEER>

SIZE
D

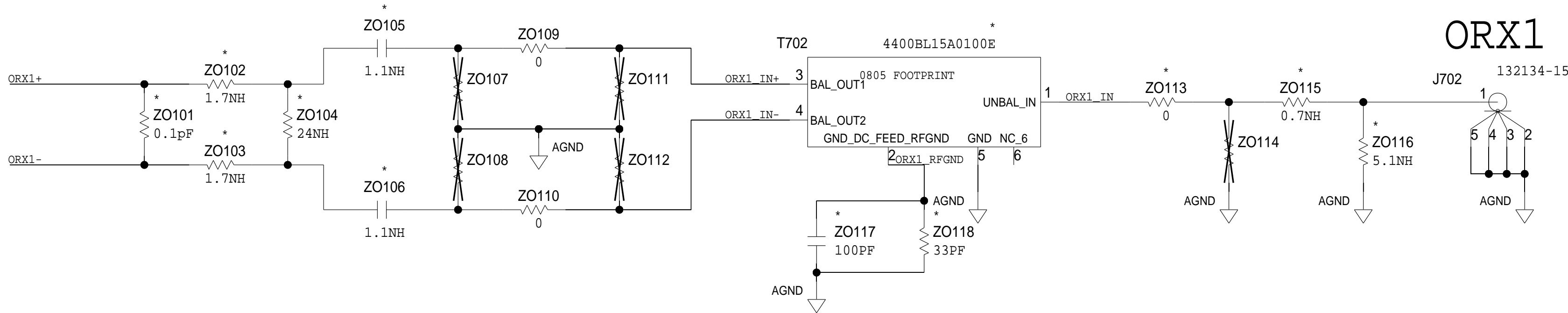
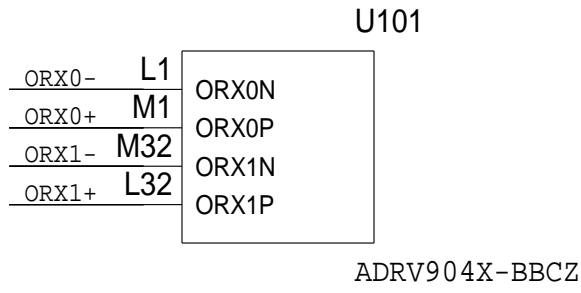
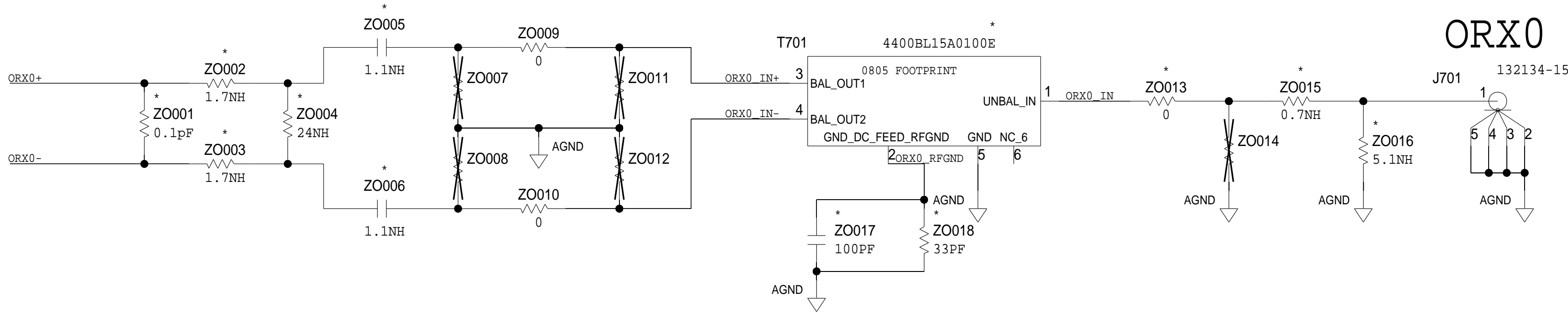
SCALE
1:1

SHEET 6 OF 19

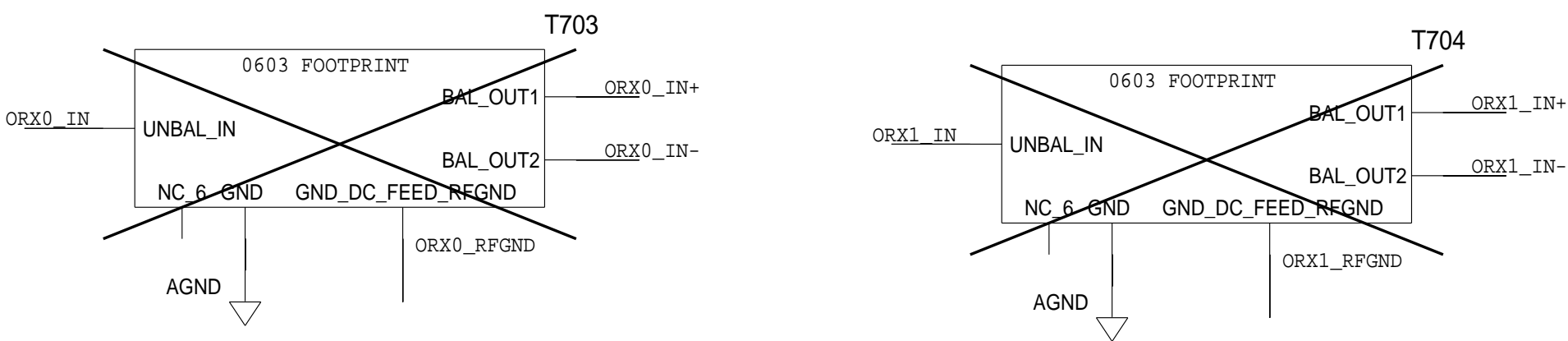
OBSERVATION RX RF INPUT

EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED



OVERLAP ORX BALUNS



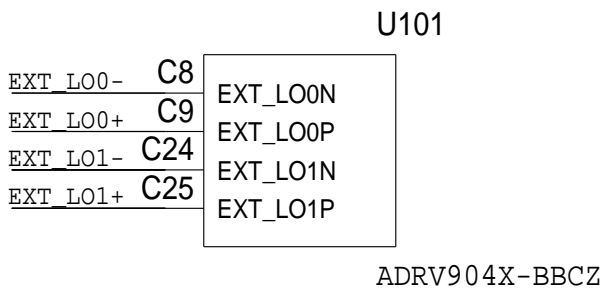
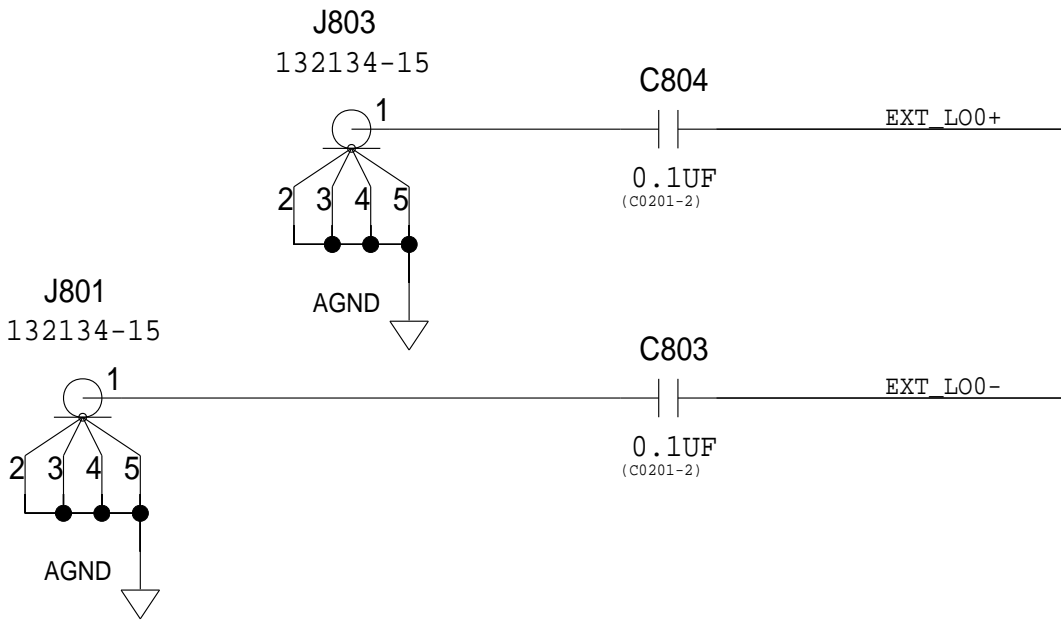
SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): ADRV904X : N/A			
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PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 7 OF 19

EXTERNAL LO IN/OUT

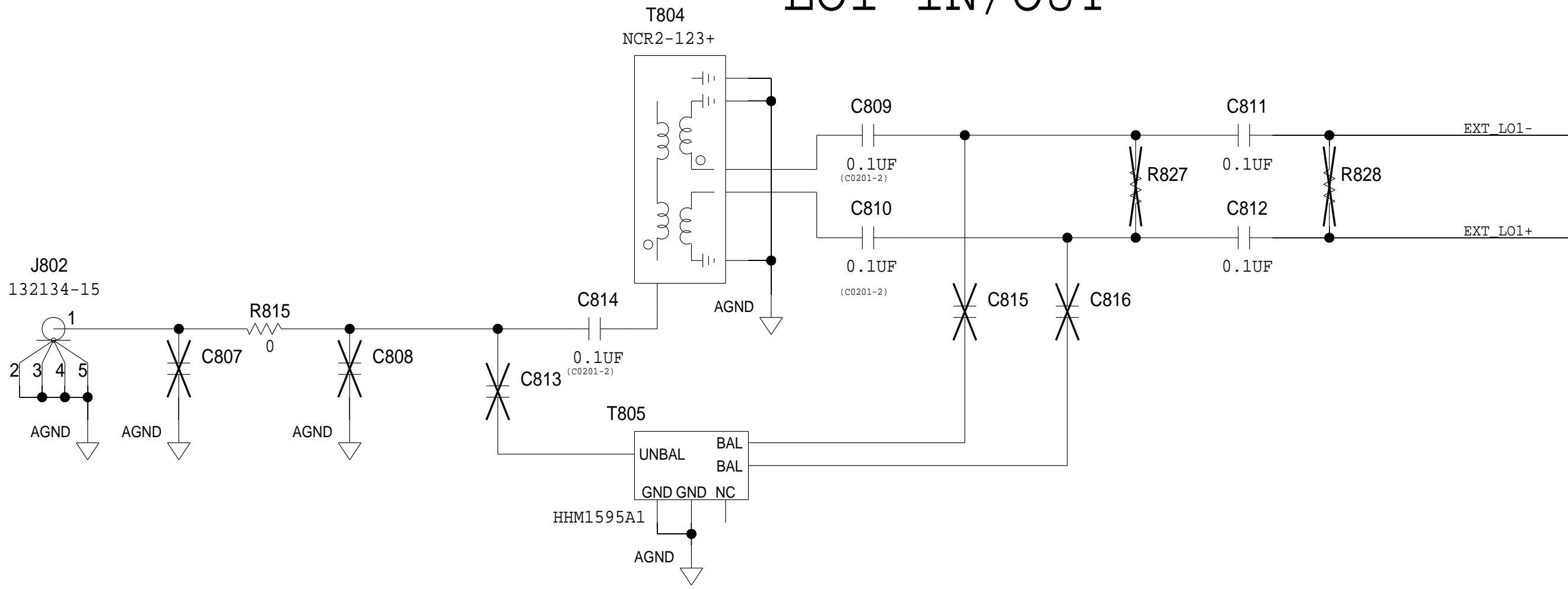
EVb MATCH HAS BEEN DESIGNED TO SUPPORT THE WIDEST MATCH POSSIBLE;
MATCHING TOPOLOGY COULD BE REDUCED/SIMPLIFIED DEPENDING ON THE SYSTEM REQUIREMENTS.

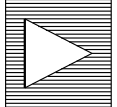
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

LO0 IN/OUT



LO1 IN/OUT



 ANALOG DEVICES	SCHEMATIC			
	HW TYPE : Customer Evaluation Product(s): ADRV904X : N/A			
	DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795		REV C
	PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 8 OF 19

CLOCK GENERATION/DISTRIBUTION

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

DEVCLK-	A15	DEVCLKN	U16
DEVCLK+	A14	DEVCLKP	U17
SYSREF-	A19	SYSREFN	EXT_CLKN
SYSREF+	A18	SYSREFP	EXT_CLKP

ADRV904X-BBCZ

DEVCLK

SYSREF

CLKPLL OUT

VCXO

SCHEMATIC



HW TYPE : Customer Evaluation
Product(s): ADRV904X
: N/A

DESIGN VIEW
<DESIGN_VIEW>
PTD ENGINEER
<PTD_ENGINEER>

DRAWING NO.
02_066795

REV
C

SIZE D SCALE 1:1 SHEET 9 OF 19

D

C

B

A

D

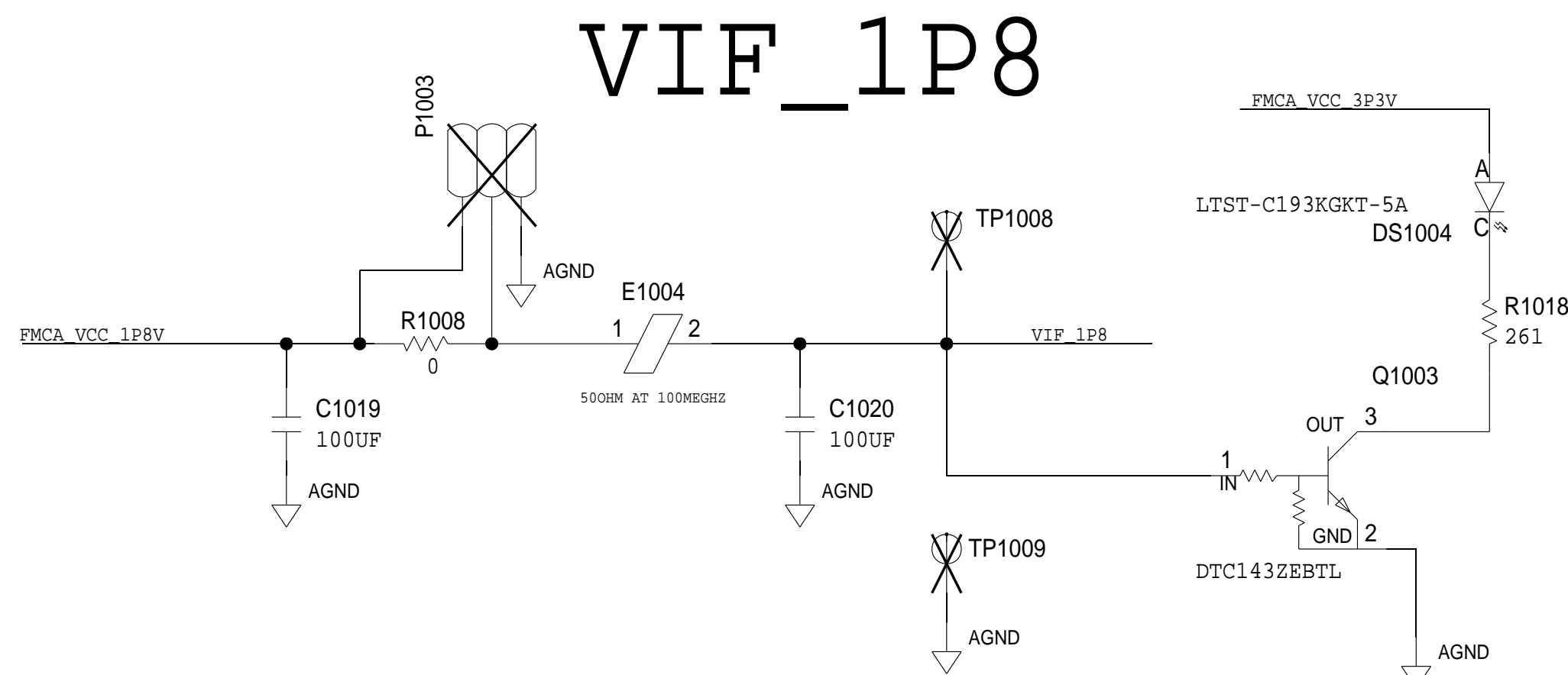
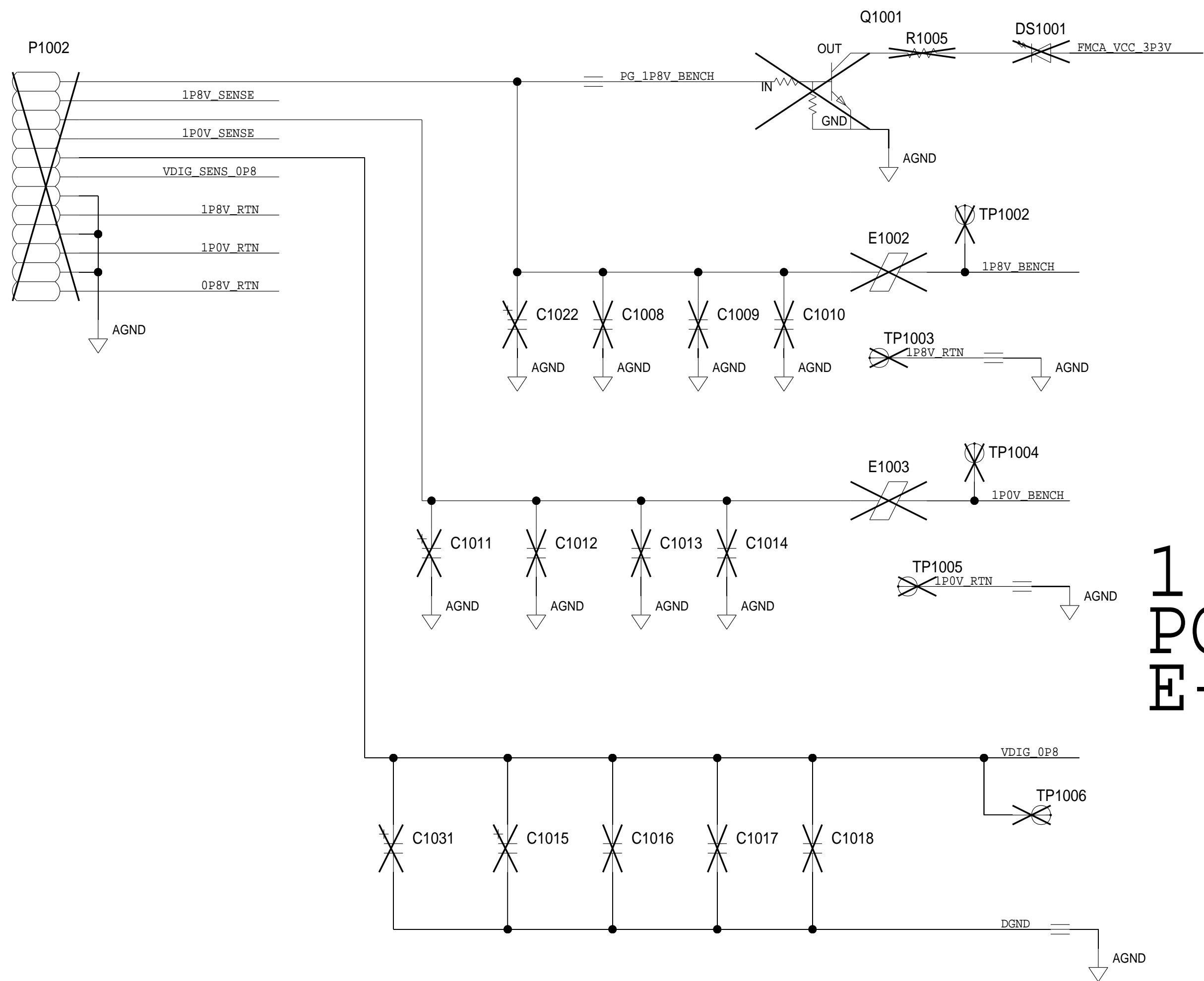
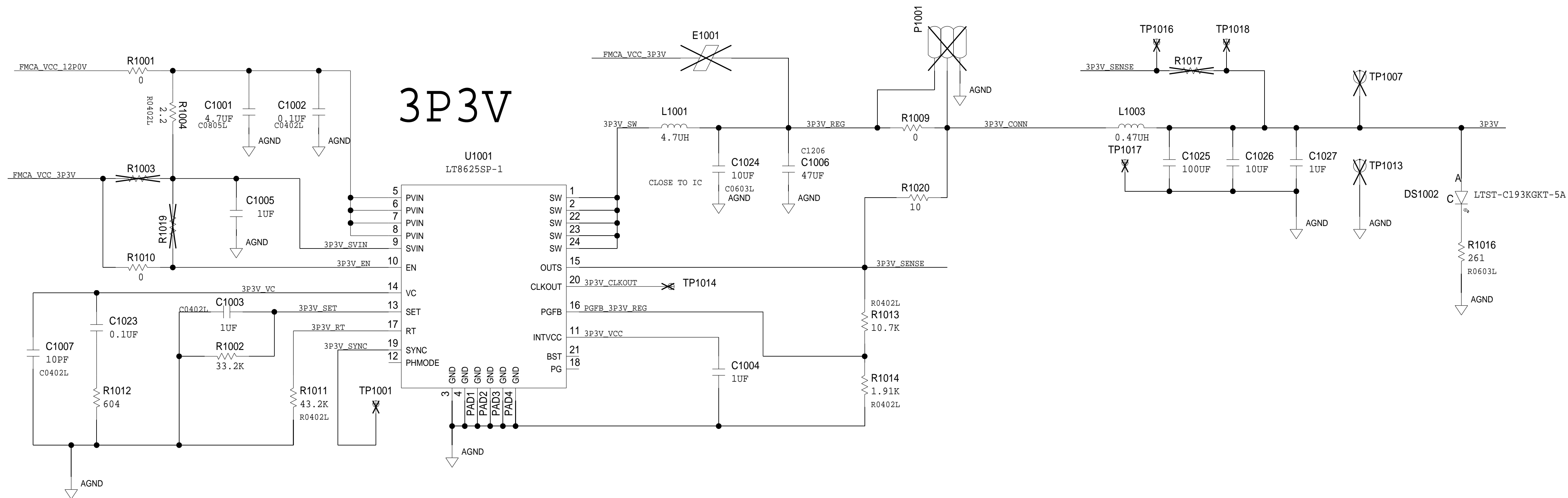
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POWER SUPPLY

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

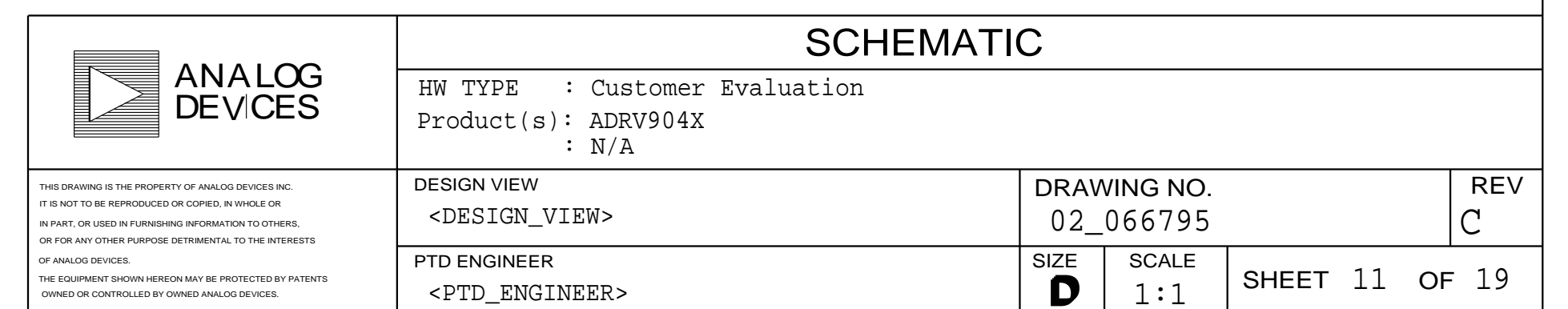
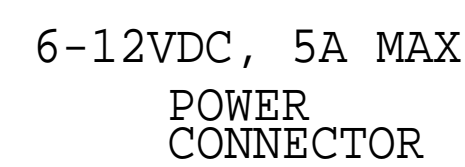


1.8V, 1.0V, 0.8V
POWER SUPPLY DUT
E-EVB

SCHEMATIC			
HW TYPE : Customer Evaluation Product(s): ADRV904X : N/A			
DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795	REV C	
PTD ENGINEER <PTD_ENGINEER>	SIZE D	SCALE 1:1	SHEET 10 OF 19

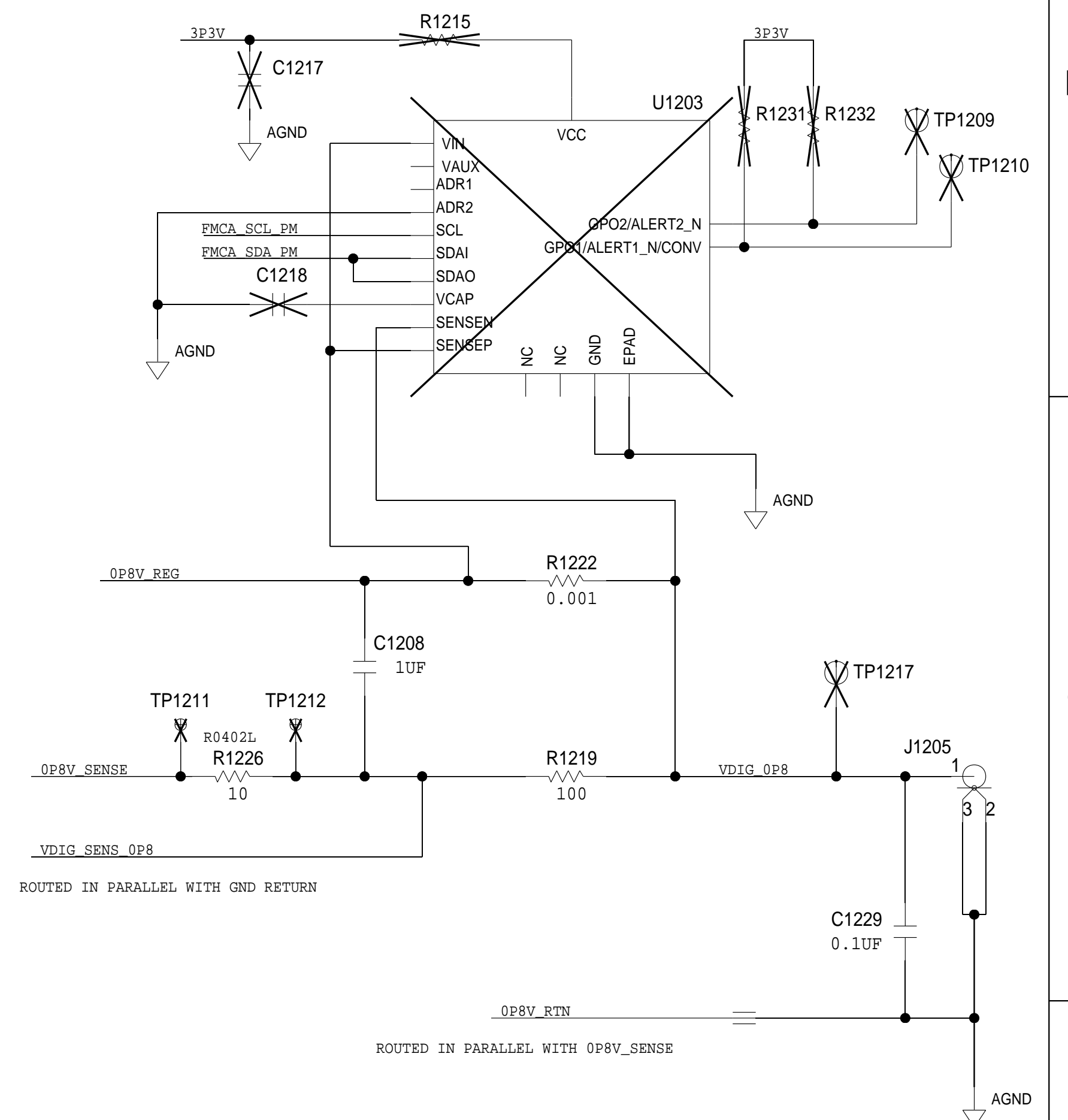
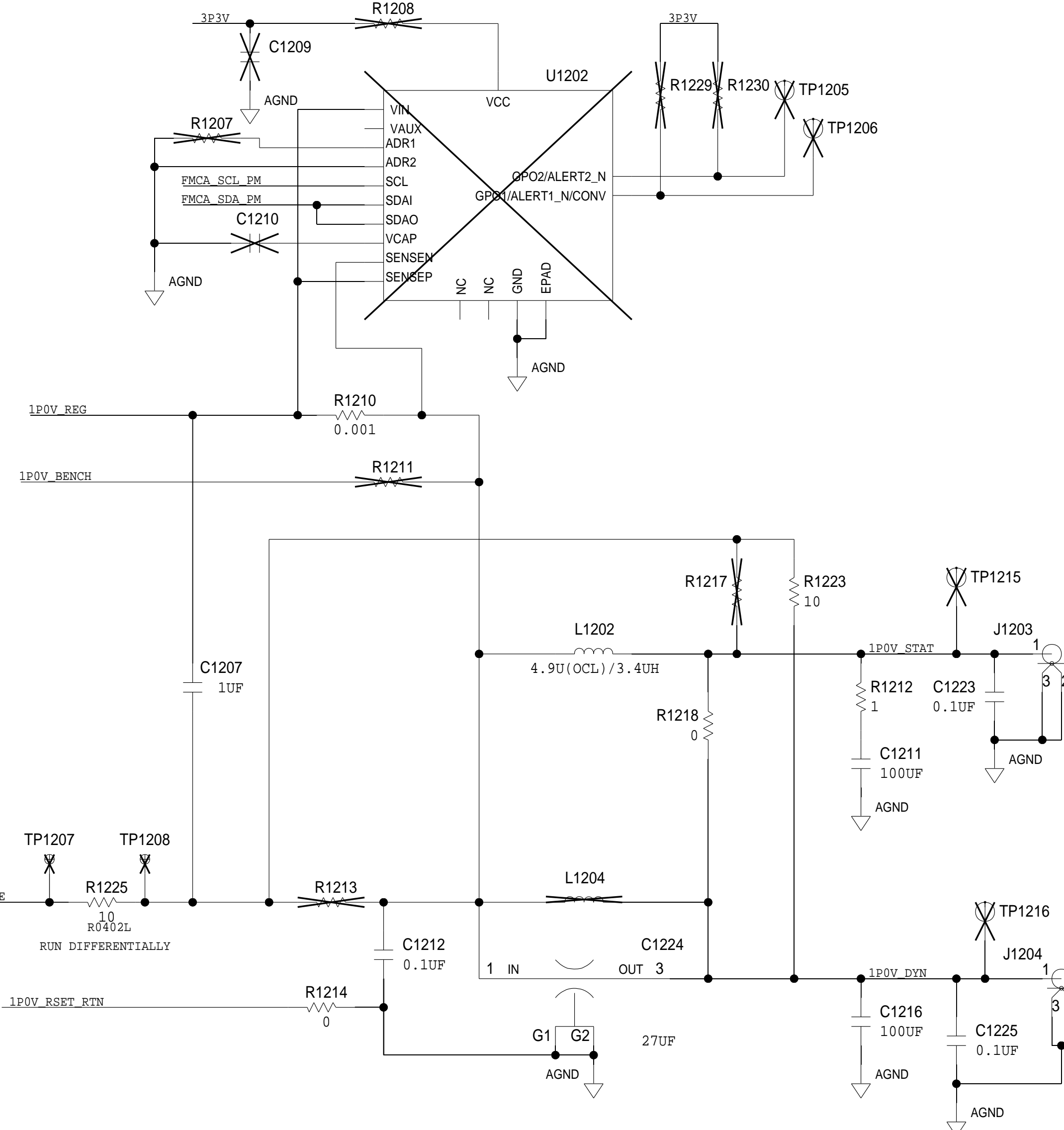
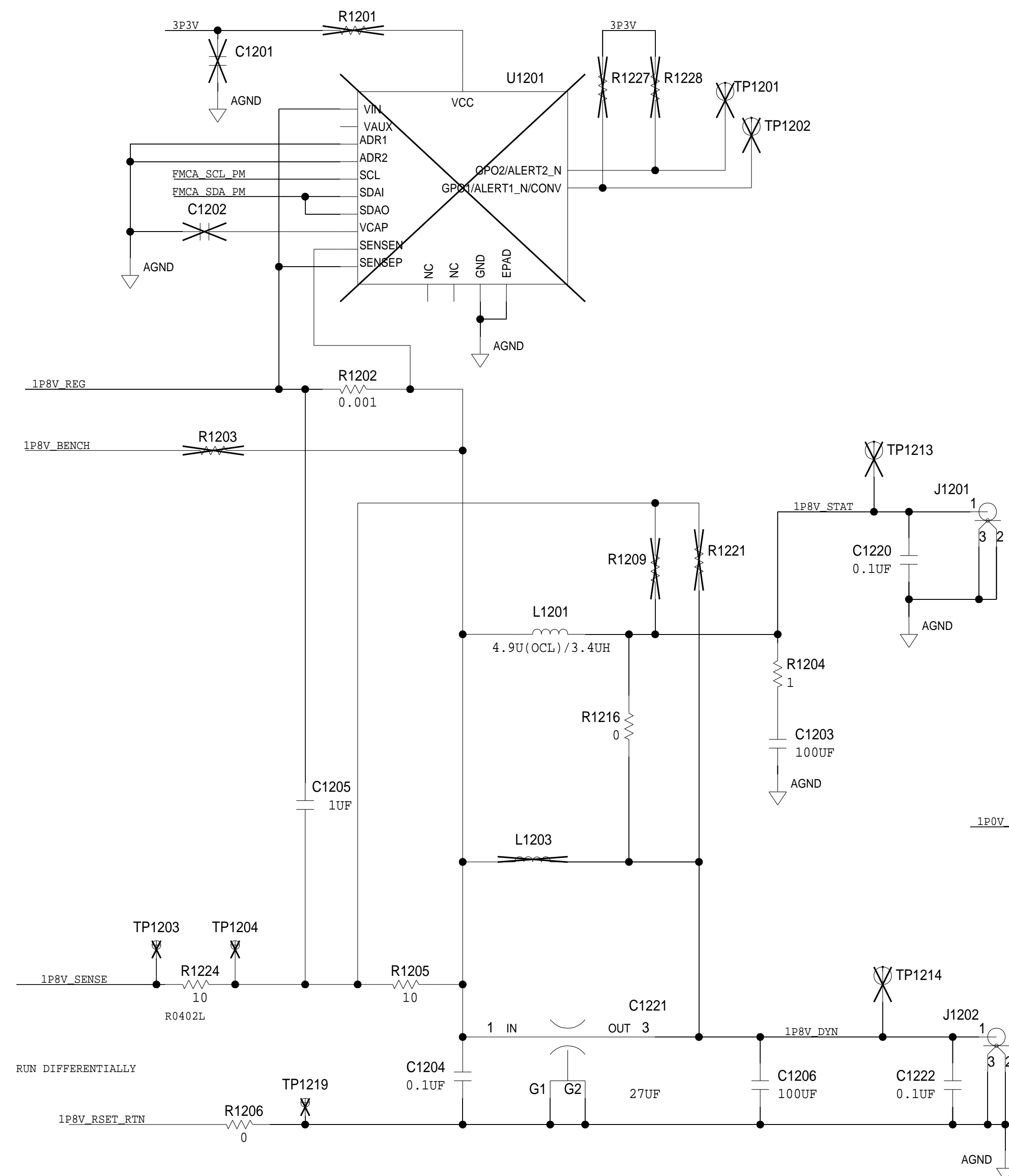
POWER SILENT SWITCHER

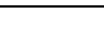
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REV	DESCRIPTION	DATE	APPROVED



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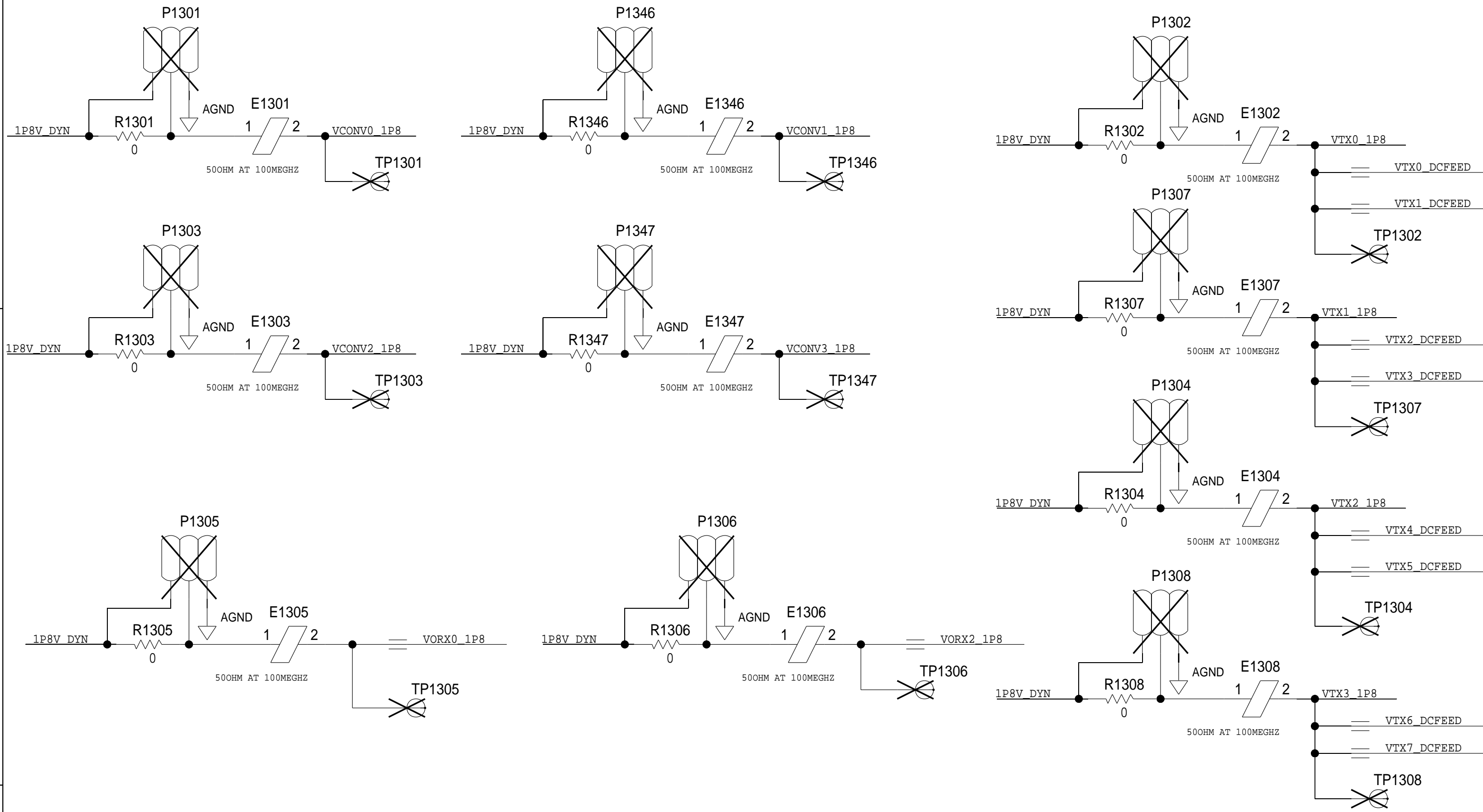
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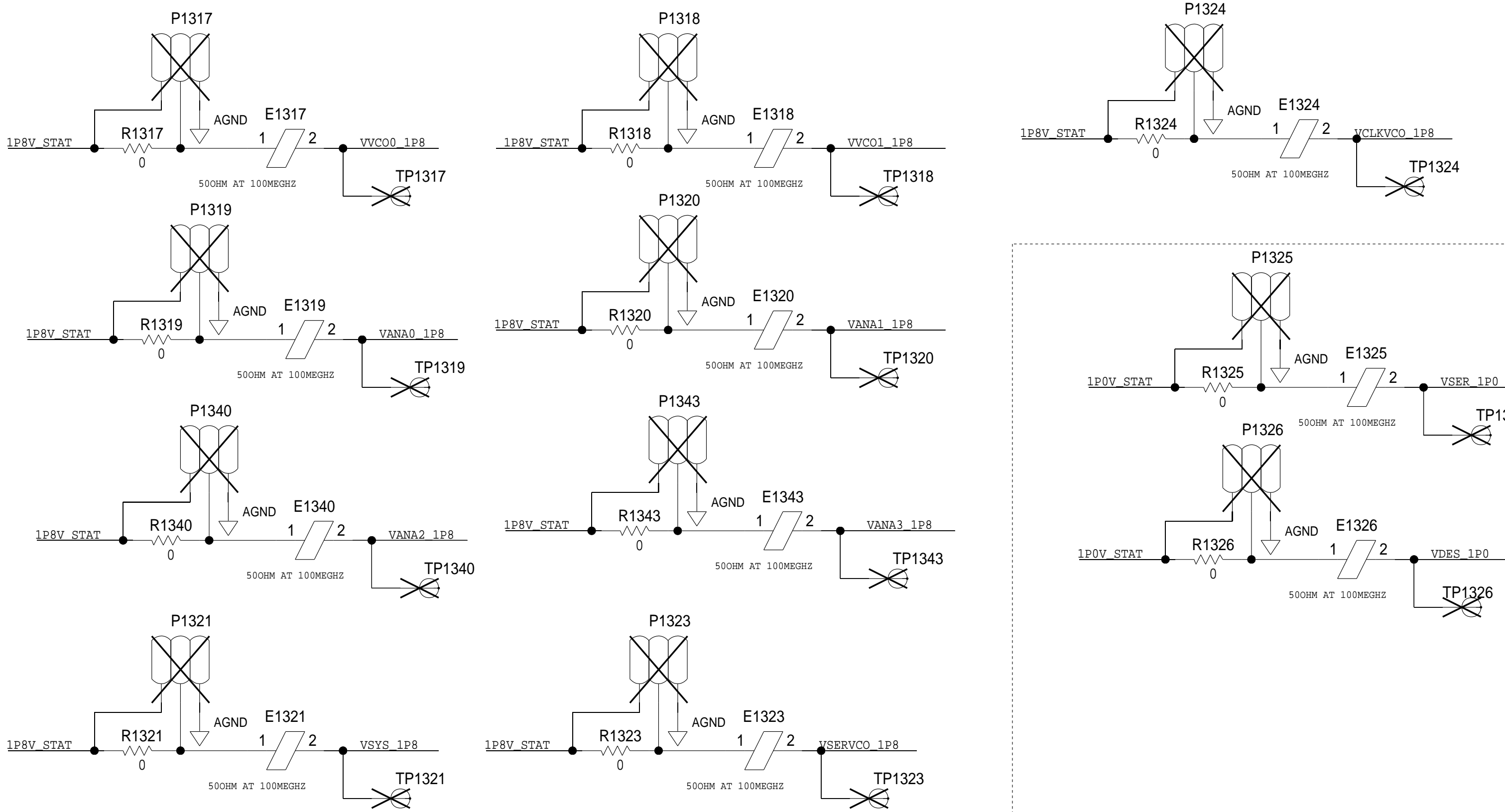
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		HW TYPE : Customer Evaluation Product(s) : ADRV904X : N/A				
<p>THIS DRAWING IS THE PROPERTY OF ANALOG DEVICES INC. IT IS NOT TO BE REPRODUCED OR COPIED, IN WHOLE OR IN PART, OR USED IN FURNISHING INFORMATION TO OTHERS, OR FOR ANY OTHER PURPOSES DEPENDANT ON THE AGREEMENTS OF ANALOG DEVICES.</p> <p>THE EQUIPMENT SHOWN HEREIN MAY BE PROTECTED BY PATENTS OWNED OR CONTROLLED BY OTHERS ANALOG DEVICES.</p>		DESIGN VIEW <DESIGN_VIEW>		DRAWING NO. 02_066795		REV C
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POWER DISTRIBUTION

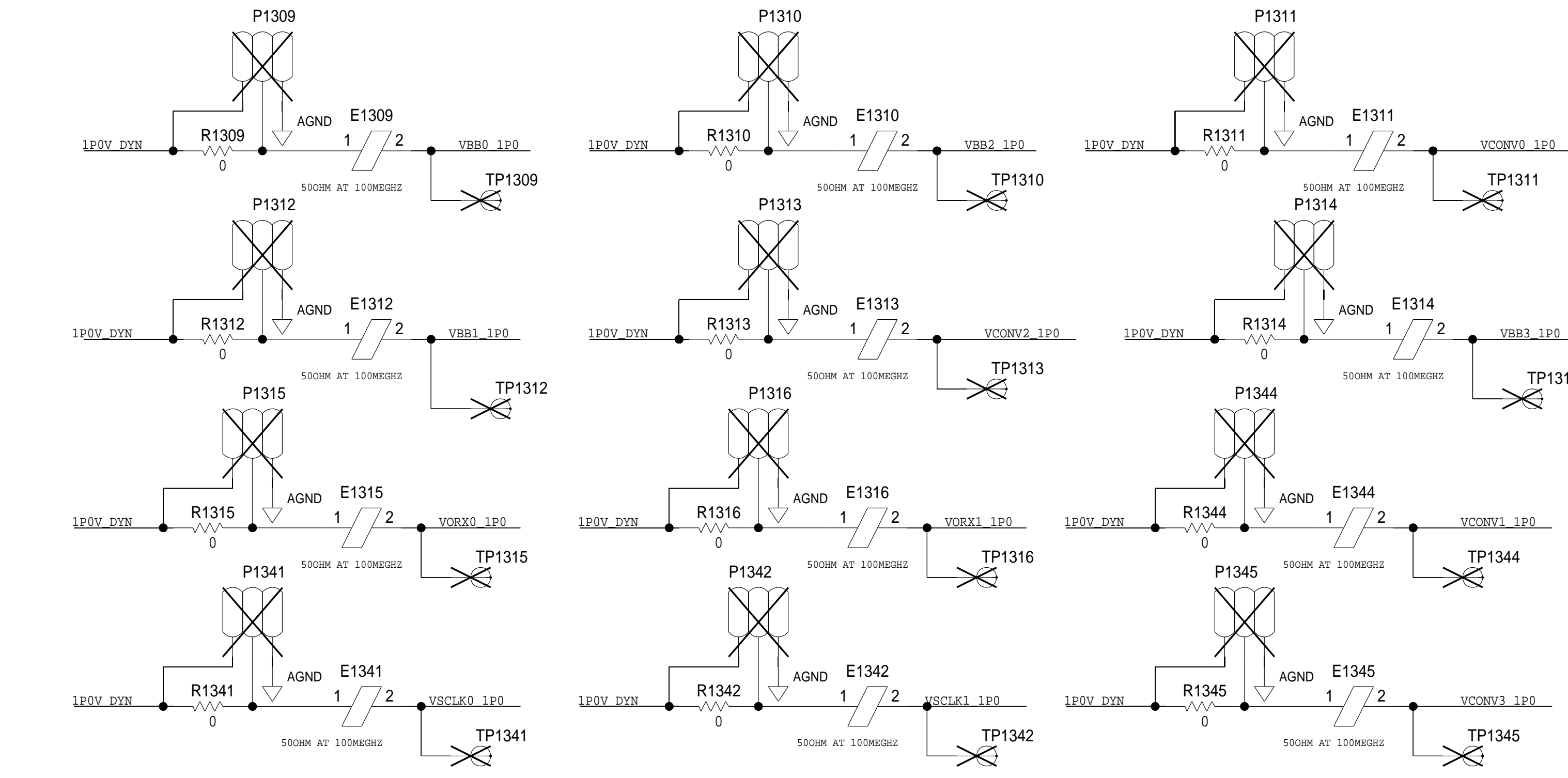
1.8V ANALOG DYNAMIC SUPPLIES



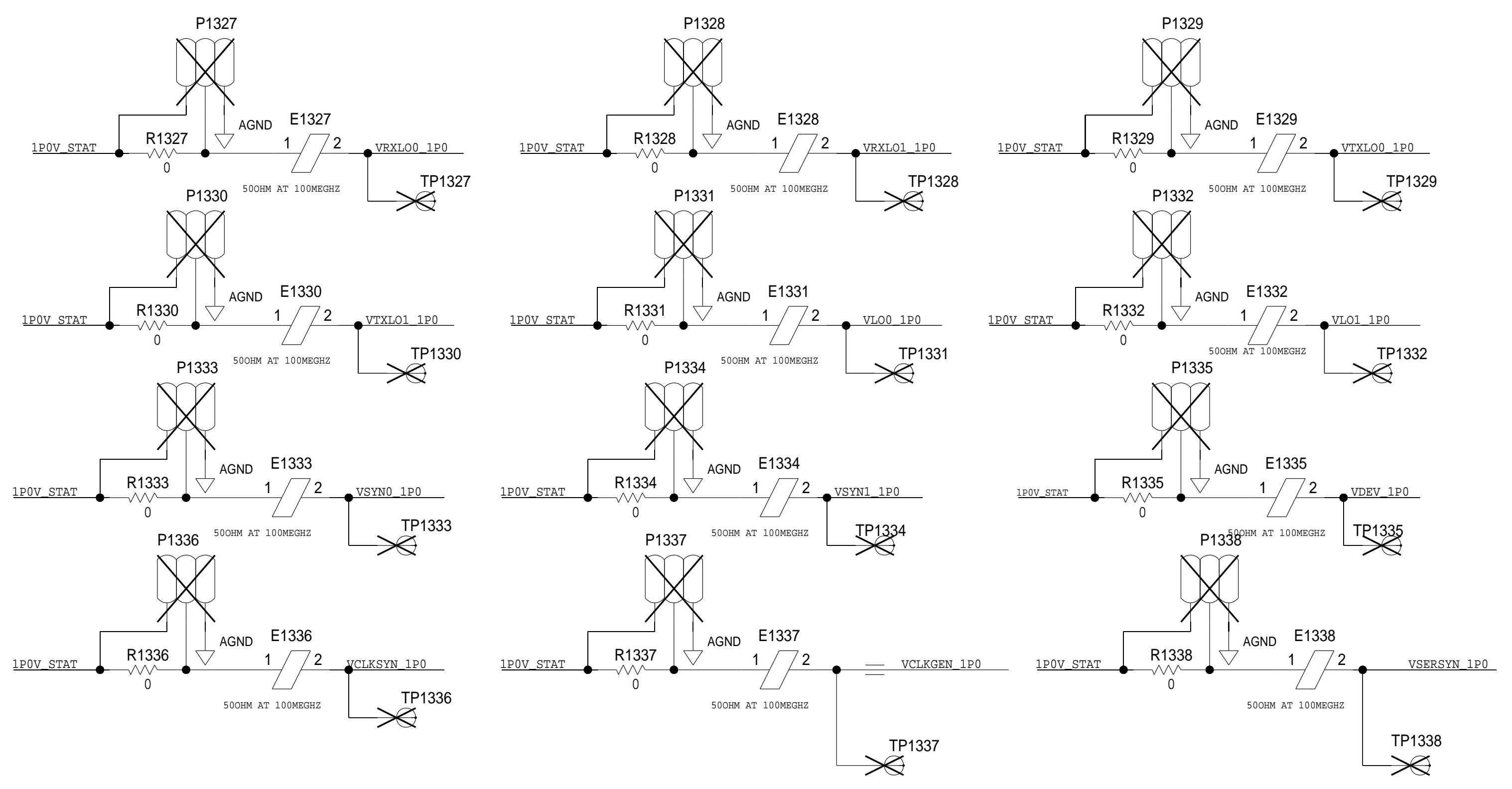
1.8V ANALOG STATIC SUPPLIES



1.0V ANALOG DYNAMIC SUPPLIES



1.0V ANALOG STATIC SUPPLIES



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DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795	REV C	
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POWER INPUT

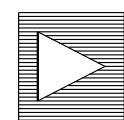
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0.8V CAPS

1.0V CAPS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED



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DEVICES

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SCHEMATIC

HW TYPE : Customer Evaluation
Product(s): ADRV904X
: N/A

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DRAWING NO.

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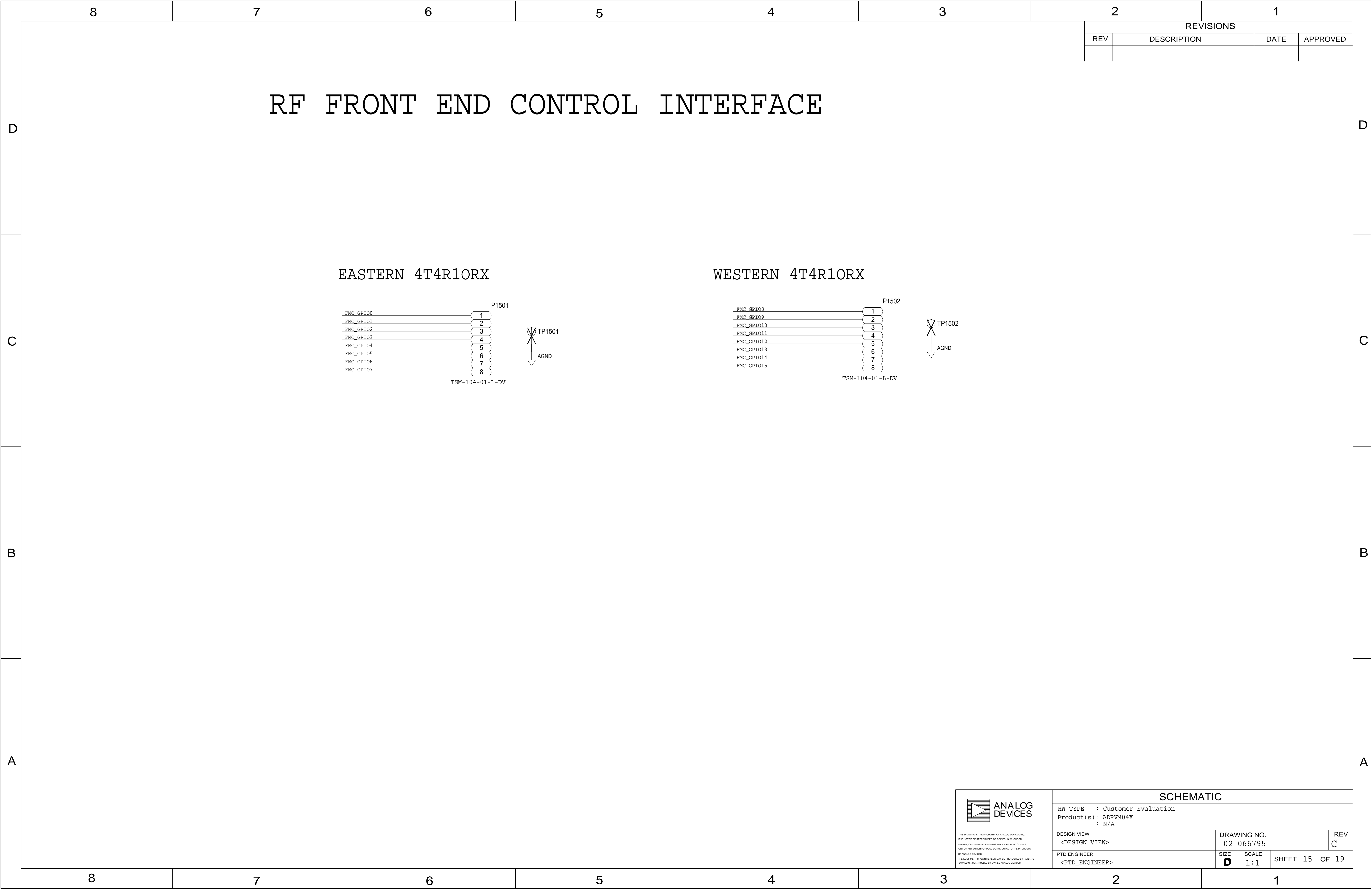
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14

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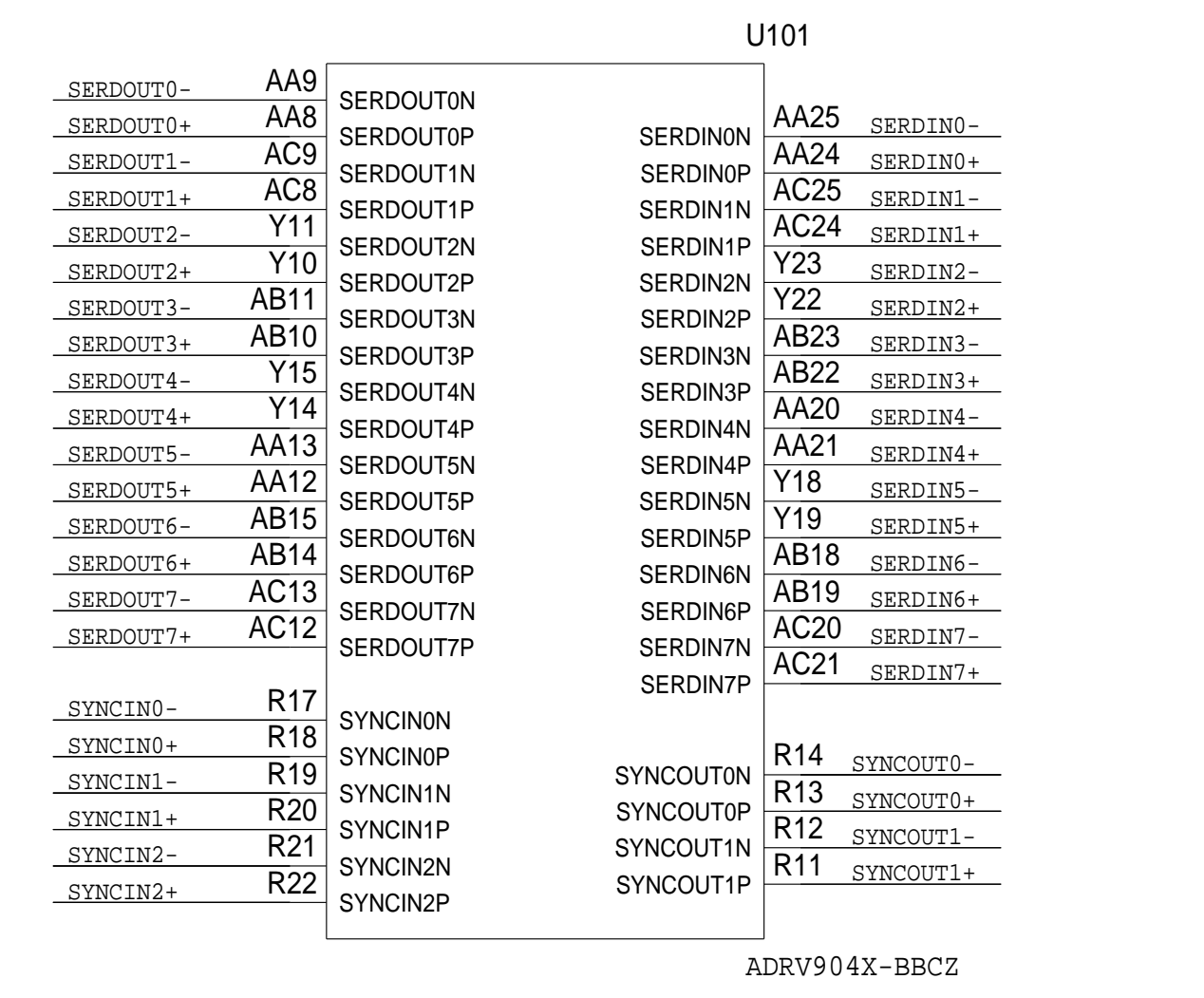
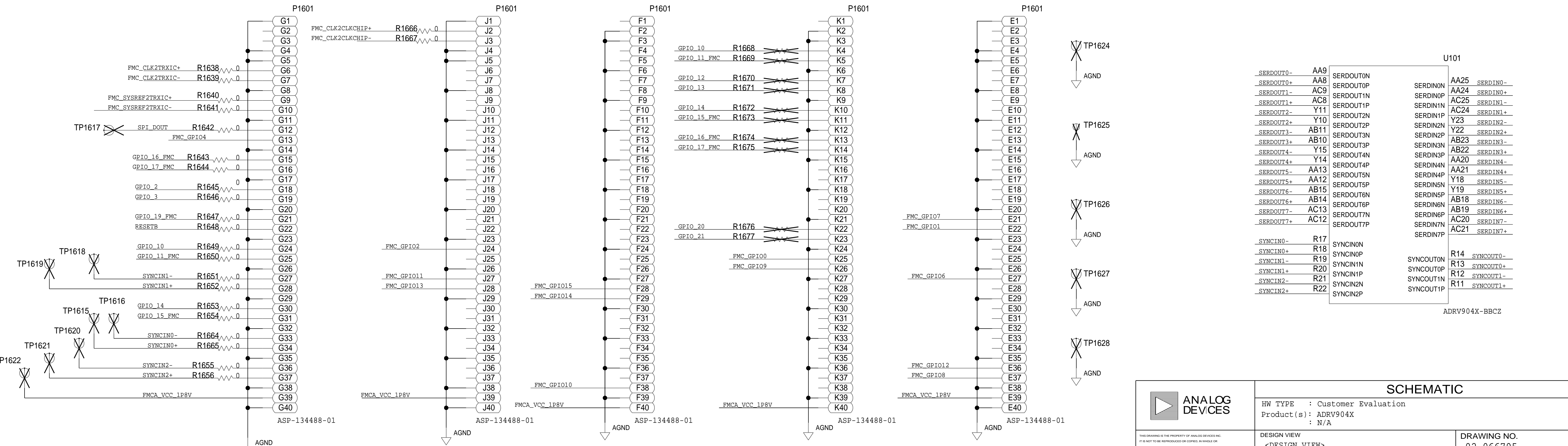
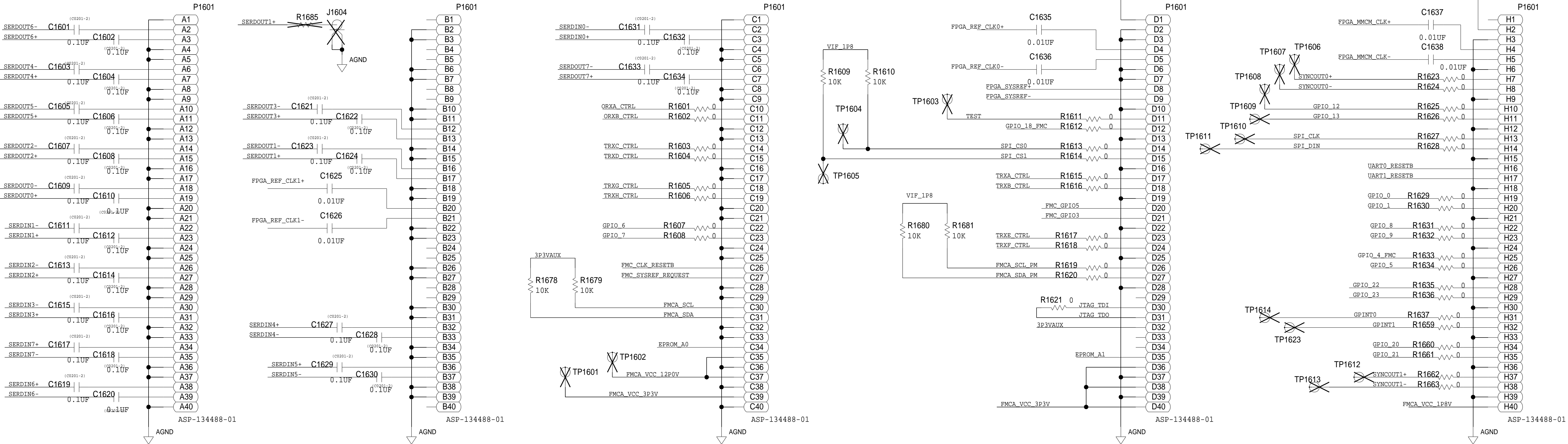
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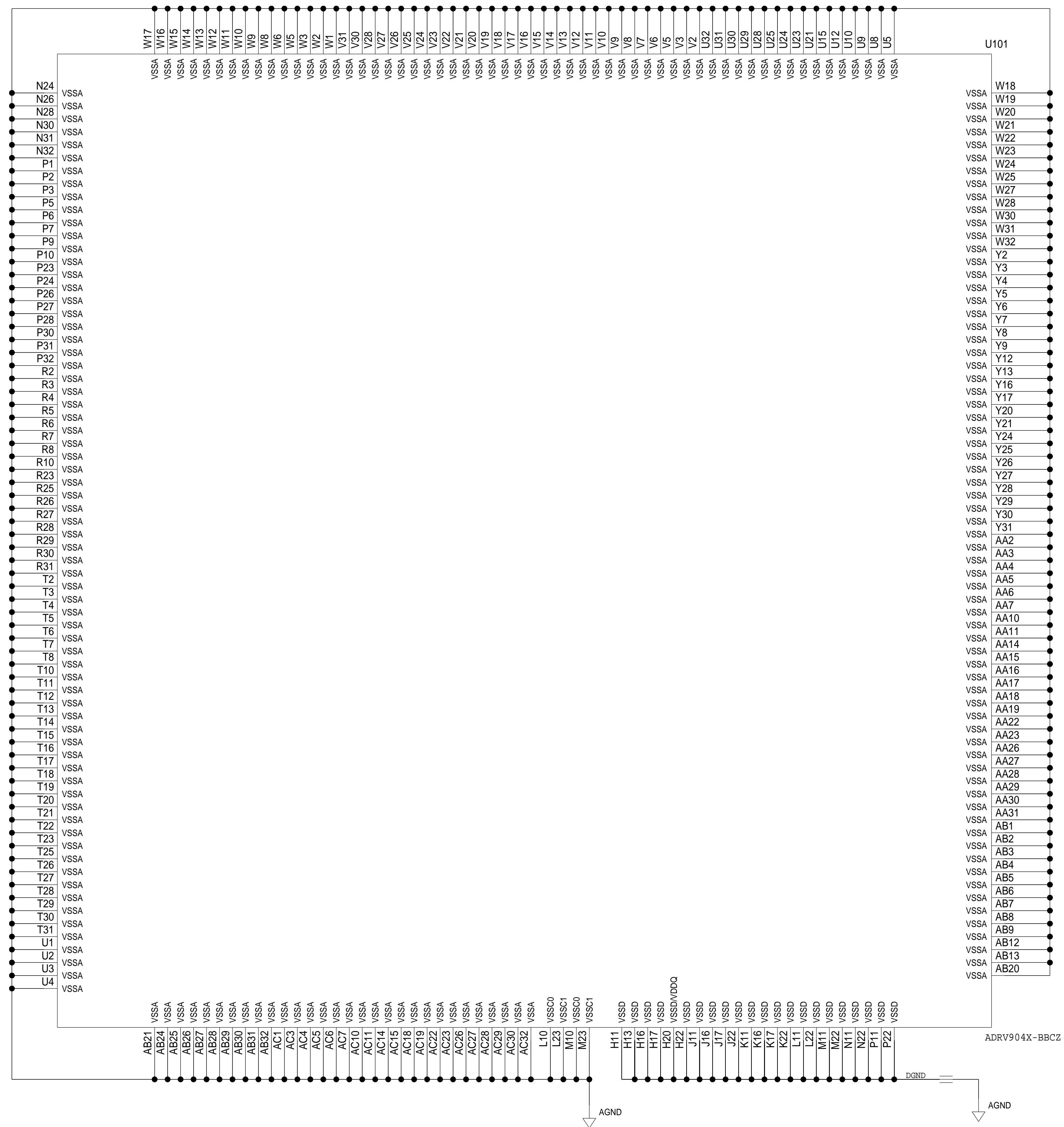


FPGA CONNECTIONS

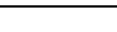
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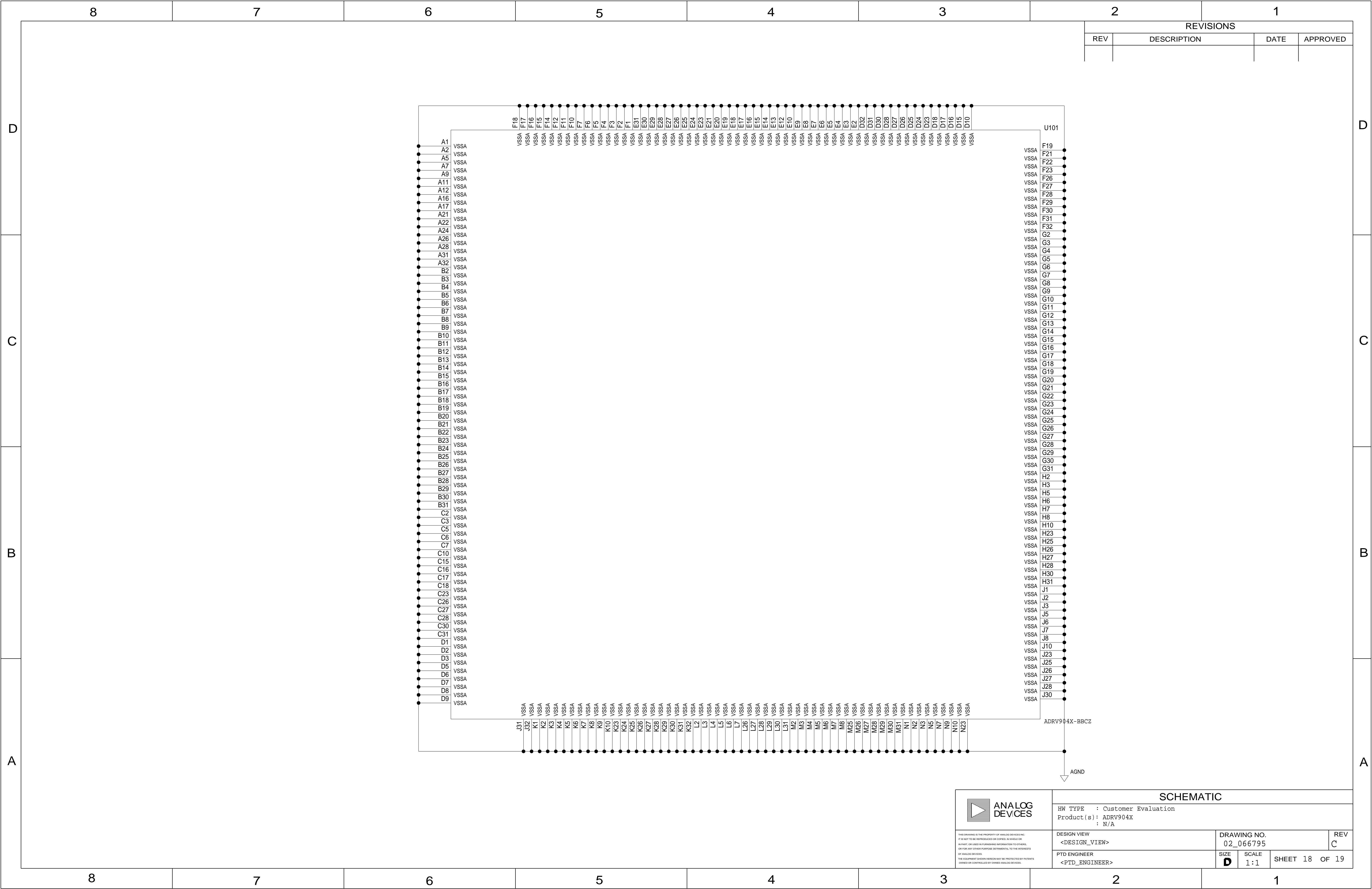


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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

 ANALOG DEVICES	SCHEMATIC			
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

SCHEMATIC			
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DESIGN VIEW <DESIGN_VIEW>	DRAWING NO. 02_066795	REV C	
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